International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 8, Issue 6, June 2021)

# Low Power Tolerant Non Volatile Lookup Table Design

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***Abstract:*** **Emerging non volatile memories (NVMs), such as PRAM, and RRAM, have been widely investigated to replace MRAM as the configuration bits in field-programmable gate arrays (FPGAs) for high security and instant power ON. This brief introduces a low-power variation-tolerant non volatile lookup table circuit to overcome the reliability issue in read and write the data. In present work large *R*OFF/*R*ON, 1T1R RRAM cell is used to provide sufficient sense margin as a configuration bit and a reference resistor. A single-stage sense amplifier with voltage clamp is employed to reduce the power and area without impairing the reliability. Evaluation shows that 22% reduction in delay, 38% reduction in power, and the tolerance of variations of 2.5× typical *R*ON or *R*OFF in reliability are achieved for proposed non volatile LUT with eight inputs.**

***Index Terms*—Logic-in-memory, low power, non-volatile lookup table (nvLUT), RRAM, variation tolerant.**

## 1. INTRODUCTION

SRAM-based field-programmable gate arrays (FPGAs) have been widely used during the last decades. However, the volatility of SRAM has limited FPGAs in applications where high security and instant power-on are required. The problem can be solved by introducing non volatile memory (NVM) as the configuration bit. The emerging non volatile memories such as PRAM, and RRAM, have been verified with better scalability and logic compatibility. Based on the logic in memory concept that is look up table design, which is the core building block in FPGAs, has been proposed with non volatility. First, various non volatile SRAM structures with and RRAM were proposed to directly replace SRAM in the traditional lookup table to acquire non volatility. However, the size of non volatile SRAM cell is remarkably larger than that of SRAM, and the write disturbance is also difficult to avoid for half-select RRAM cells, and also proposed eight input LUT.

## 2. SYSTEM DESIGN

### *Existing System*

In existing system Magneto resistive random access memory(MRAM) is used as configuration bit. Configuration bits are received in serially from external memory in the power down case, then data will be loss in this case. In order to use this memory the inconsistency has been introduced in the implementation of look up table.

### *Drawbacks*

- The resistance state of MRAM (Magneto resistive random access memory) is small compare with RRAM to store the data in the form of resistance state in storage cell of a MRAM ,thus resulting in larger area due to serial parallel magnetic junctions .
- Roff/Ron for MRAM which results in less sense margin and larger area.

### *Proposed System*

Proposed system will be developed on **resistive** random access memory (resistive RAM), that can modify the structure of a storage cell. RRAM cell is employed as a configuration bit to provide sufficient sense margin .In proposed design, the nvLUT presented as shown in Fig. 1. The input is all too easily be extended to eight in the current products.

### *Advantages*

- RRAM(Resistive random access memory) has larger Roff/Ron(Resistance state) ratio to store the data in their storage cell .
- RRAM cell has been used as the configuration bit inproposed and a reference resistor as been used to provide sufficient sense margin to read and write data.
- The area cost is decreased because no serial and parallel memory cell combinations are needed.

## 3. LOW POWER VARIATION TOLERANT NVLUT

To illustrate the design, the input nvLUT presented as shown in Fig.1, the input count is even easier FPGA products in the main stream of the six, expanded. Of the total construction nvLUT a SSAVC, a tree Multiplexer (TMUX), a MRP, a RRAM piece, and will have an footer transistor. RRAM as a reference resistor blanks at the right-most slice of the RRAM cell configuration forms for the left and four 1T1R RRAM cells. The truth table logic voltage SRAM is different from the resistance of the state, ROFF or RON, will be stored in the form of a piece of RRAM. For example, a NOR gate, in order to nvLUT program, R0 RON 1, as indicated, R1, R2, and R3 ROFF represents 0. The inputs IN0 and IN1 TMUX of

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the RRAM cell to select the program to the program. RRT in the sense amplifier to the output 1 to be exposed to high parasitic RC bit and reference resistor, making the configuration of the memory margin between the resistance variation is subtle, reference may be slowDischarge path.

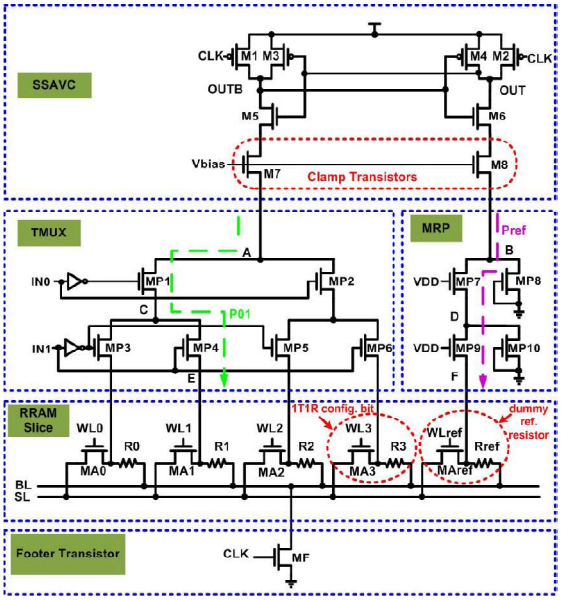


Figure:1 Architecture oflow power variation tolerant NVLUT

### *A.RRAM as configuration bit*

The 1T1R RRAM cell is employed as a configuration bit and a reference resistor to provide sufficient sense margin, Different from crossbar array, a 1T1R RRAM cell can eliminate the sneaking current and the disturbances during write and read, thus saving power and acquiring high yield. The typical RON and ROFF of RRAM are of kilo-ohms and mega ohms, respectively,and ROFF/RON is over 100, which is at least 40× larger than that of MRAM. Therefore, sufficient sense margin is guaranteed and the configuration resources are also saved by half compared with the parallel or serial combination scheme. Moreover, the RRAM storage layer

### *B. Single Stage Sense Amplifier With Voltage Clamp:*

Single Stage Sense Amplifier With Voltage Clamp converts the resistance state of RRAM into a rail-to-rail logic voltage. transistors M3–M6 constitute of a latch amplifier. Transistors M1 and M2 are used to recharge the output nodes OUT and OUTB to *V*DD .when CLK is low and transistor MF is used to initiate the conversion when CLK is high. Compared with the previous two-stage sense amplifier , the single-stage realization occupies less die area. The internal voltages in TMUX and MRP are clamped to lower voltages by the clamp transistors to save power.

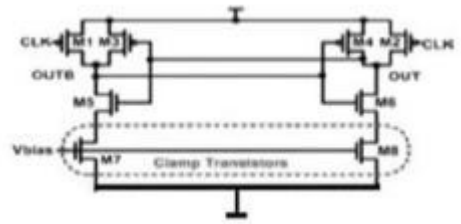


Figure 2: Single Stage Sense Amplifier with Voltage Clamp

It has low power dissipation and a sense of basic differential amplifier in comparison to theoffset voltage. The differential voltage sensing operation, providing fast loading equipment forsimultaneous exchange of meaning is the primary purpose of the amplifier. SSAVC rail-to-railvoltage logic state changes the resistance of the RRAM

In previous work, the inner nodes of the selected path in multiplexer and reference path are both pre charged to *V*DD or (*V*DD-*V* th) when CLK is low . The charges are discharged to a capacitor or ground when CLK is high, resulting in considerable power waste. To alleviate this issue, transistors M7 and M8 are inserted between the sense amplifier and the TMUX/MRP. By applying a proper clamp voltage *V*bias, which is lower than *V*DD, on the gates of M7 and M8, the inner nodes of the selected path in TMUX and MRP can only be pre charged to (*V* bias-*V* th). In an FPGA chip, *V* bias for different non volatile LUTs can be generated by a single voltage regulator with negligible overhead and it can also be tuned for different PVT conditions.

### *C. Tree Multiplexer (TMUX)*

TMUX is a multiplexer with select line in0 and in1 which are used to select the corresponding RRAM. Its working principle issimilar to NOR operation. It is a major dynamic power reductiontechnique. Gate the clock as much as the flop is not necessary to be toggled. Otherwise in every clock cycle flop will toggle, dissipate more power.

Table: 1 NOR operation in TMUX

| IN0 | IN1 | OUT |
|---|---|---|
| 0 | 0 | R0 |
| 0 | 1 | R1 |
| 1 | 0 | R2 |
| 1 | 1 | R3 |

This brief introduces low power variation tolerant nvLUT to overcome the previous work
Because

- Area cost is decreased because no Serial parallel memory cell is used
- Large R OFF/R ON

### *D. Matched Reference Path*

The MRP is devised to minimize the parasitic *RC* mismatch between the above-mentioned two paths. To illustrate this point, IN0 and IN1 are assumed to take the logic values of 0 and 1, respectively. As shown in Fig. 1, the path marked by

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the green dash line in TMUX, P01, is selected to be compared with the reference path, *P*ref . For reliable sensing, the parasitic *RC*s of P01and *P*ref should be equivalent. Therefore, the transistors MP8 and MP10 with their gate grounded are, respectively, added at the nodes B and D in MRP to imitate the parasitic effects of off-state transistors MP2 and MP3 at the nodes A and C in TMUX.

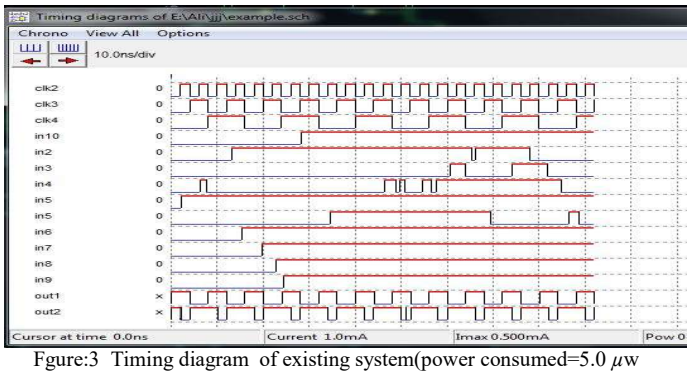
### *E. Footer Transistor*

The function of footer transistor MF is to allow current to flow during sensing and it is closed during precharge to restrain leakage.

### *F.RRAM slice*

- It constitutes of four RRAM cellsat the left for configuration and a dummy RRAM cell at the right most as a reference resistor
- Because of the quadratic relationship between energy and voltage, considerable average power saving can be achieved by the reduction of pre charge voltage.
- Although the voltage clamp may incur reduced currents into the sense amplifier

## 4. SIMULATION RESULTS




Fgure:3 Timing diagram of existing system(power consumed=5.0 $\mu$w

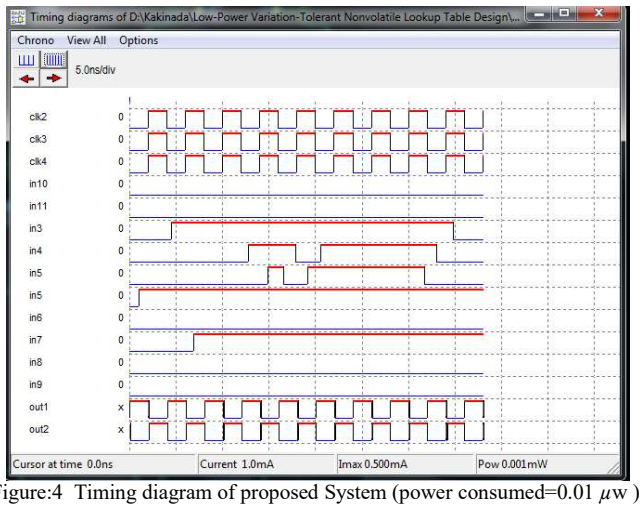



Figure:4 Timing diagram of proposed System (power consumed=0.01 $\mu$w )

Figure:5 Simulation result of proposed system (power consumed=57.3 $\mu$w)

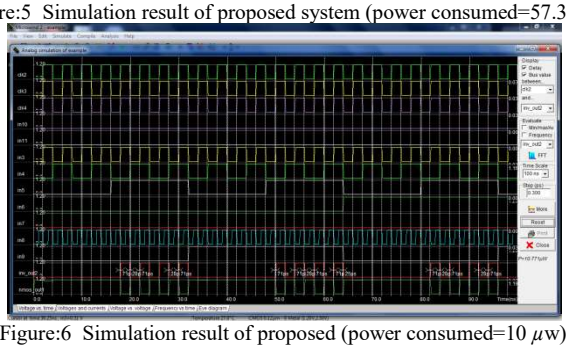
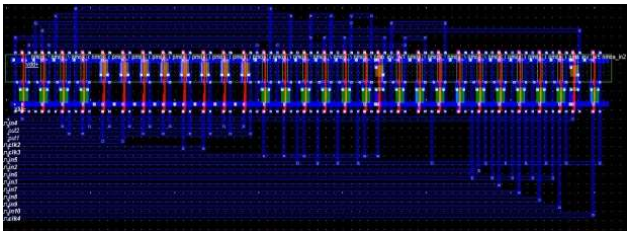


Figure:6 Simulation result of proposed (power consumed=10 $\mu$w)



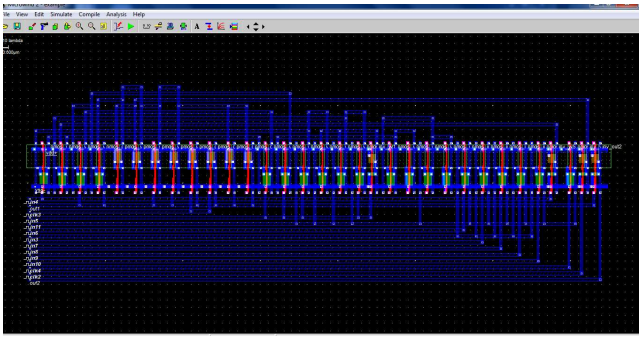


Figure:8 Layout diagrams of existing and proposed system

## 5. SOFTWARE REQUIREMENTS

In this the circuits can be designed and compel hear using verilog file. Micro wind automatically generate a error free cmos layout although this place rout is not optimized enough as we do not indulge in complex place and route algorithm and also create cmos layout of their own compile one line verilog syntax or custom build the layout by manual drawing. DSCH can convert the digital circuit into verilog file which can be further synthesised for FPGA/CPLD devices of any vendor. the same verilog file can be compiled for layout conversation in micro wind DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH provides a user-friendly environment

for hierarchical logic design, and fast simulation with delay analysis, which allows the design and validation of complex circuits

**Tools of Micro wind:**

- Micro wind
- DSCH
- Microwind3 Editor
- Micro wind 2D viewer
- Micro wind 3D viewer
- Micro wind analog simulator
- Micro wind tutorial on MOS devices
- View of Silicon Atoms

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