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32 Bit High Speed Vedic Multiplier using Vedic Mathematices

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***Abstract*: The planning of high speed religious text multiplier factor mistreatment the techniques of Ancient Indian religious text arithmetic that are changed to enhance performance. religious text arithmetic is that the ancient system of arithmetic that incorporates a distinctive technique of calculations supported sixteen Sutras. The work has proved the potency of Urdhva Triyagbhyam– religious text technique for multiplication that strikes a distinction within the actual method of multiplication itself. It permits parallel generation of intermediate merchandise, eliminates unwanted multiplication steps and scaled to higher bit levels.**
Urdhva tiryakbhyam Sanskrit literature is most effective Sanskrit literature (Algorithm), giving minimum delay for multiplication of all kinds of numbers, either little or massive.

***Key words*- Xilinx twelve.1i tool, Sparton 3E kit**

I. INTRODUCTION

Multiplication is a vital basic perform in arithmetic operations. Multiplication-based operations like Multiply and Accumulate(MAC) and real number ar among a number of the ofttimes used Computation- Intensive Arithmetic Functions(CIAF). Currently, multiplication time remains the dominant think about determinative the instruction cycle time of a DSP chip. thus there's a desire of high speed multiplier factor.

The demand for prime speed process has been increasing as a results of increasing laptop and signal process applications. Higher turnout arithmetic operations ar necessary to attain the required performance in several period signal and image process applications [2]. one in all the key arithmetic operations in such applications is multiplication and also the development of quick multiplier factor circuit has been a theme of interest over decades. Reducing the time delay and power consumption ar terribly essential necessities for several applications. This work presents totally different multiplier factor architectures. multiplier factor supported religious text arithmetic is one in all the quick and low power multiplier factor. This improvement includes the technology wont to implement the digital circuits, the circuit vogue and topology, the design for implementing the circuits and at the best level the algorithms that ar being enforced.

II. EXISTING SYSTEM

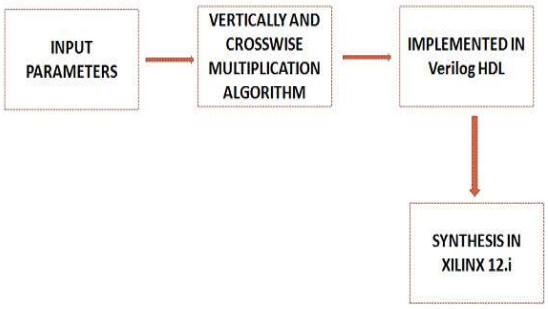
- In arithmetic logic unit multiplication is one in all the foremost advanced processes. as a result of we've got to perform the 3 operations multiplication, addition and shifting.
- When operations ar performed in serial manner delay is will increase and system potency decreases.

III. PROPOSED SYSTEM

- Multiplier supported religious text arithmetic is one in all the quick and low power multiplier factor.
- This Sanskrit literature conjointly shows the effectiveness of to cut back the NXN multiplier factor structure into associate degree economical 4X4 multiplier factor structures.

The projected multiplications were enforced mistreatment 2 totally different cryptography techniques viz. typical shift & add and religious text technique for four, 8, 16, and thirty two bit multipliers. it's evident that there's a substantial increase in speed of the religious text design

Block Diagram:



IV. WORK DONE

Vedic arithmetic is an element of 4 Vedas (books of wisdom). It offers rationalization of many mathematical terms as well as arithmetic, pure mathematics (planeco-ordinate), trig, quadratic equations, factoring and even calculus.
The word "Vedic" springs from the word "veda" which implies the store-house of all information. religious text arithmetic is especially supported sixteen Sutras (or

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aphorisms) addressing numerous branches of arithmetic like arithmetic, algebra, pure mathematics etc. These Sutras beside their temporary meanings ar noncommissioned below alphabetically.

1. (Anurupye) Shunyamanyat – If one is in magnitude relation, the opposite is zero.
2. Chalana-Kalanabyham – variations and Similarities.
3. Ekadhikina Purvena – By an extra than the previous One.
4. Ekanyunena Purvena – By one but the previous one.
5. Gunakasamuchyah – The factors of the add is adequate to the add of the factors.
6. Gunitasamuchyah – the merchandise of the add is adequate to the add of the merchandise.
7. Nikhilam Navatashcaramam Dashatah – All from nine and last from ten.
8. Shunyam Saamyasamuccaye – once the add is that the same that add is zero.
9. Sopaantyadvayamantyam – the last word and doubly the penultimate.

The projected religious text multiplier factor is predicated on the algorithmic rule Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian religious text arithmetic. These Sanskrit literature are historically used for the multiplication of 2 numbers within the decimal numeration system. during this work, we tend to apply a similar ideas to the binary numeration system to create the projected algorithmic rule compatible with the digital hardware.

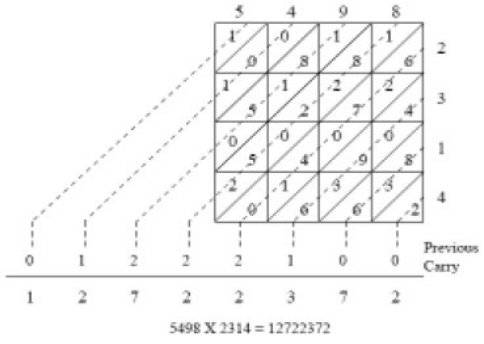

Fig (a): Example for multiplication of two numbers in the decimal number system using Urdhva Tiryakbhyam algorithm

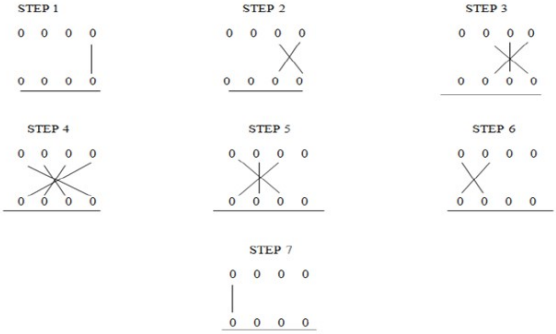

Fig (b): Example for multiplication of 2 Four-bit numbers using Urdhva Tiryakbhyam algorithm.

V. IMPLIMENTATION

The projected multiplications were enforced mistreatment religious text technique for eight, 16, and thirty two bit multipliers.

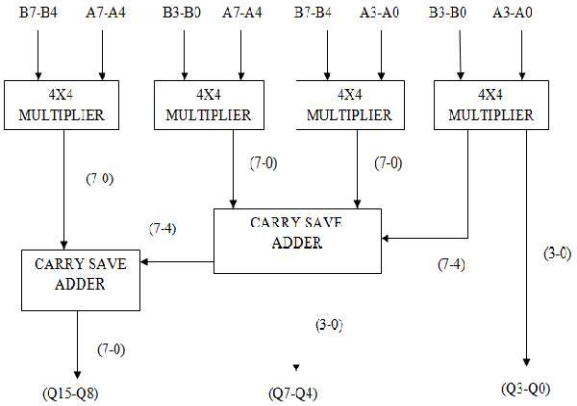

Fig (c): Implementation of 8X8 bit religious text multiplier factor RESULT → (Q15-Q8) & (Q7-Q4) & (Q3-Q0)

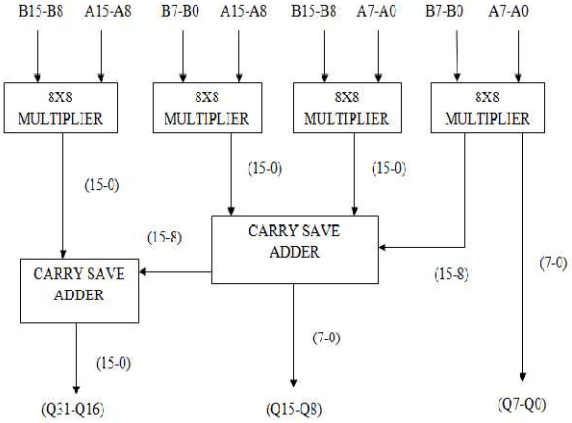

Fig (d): Implementation of 16X16 bit religious text multiplier factor RESULT → (Q31-Q16) & (Q15-Q8) & (Q7-Q0)

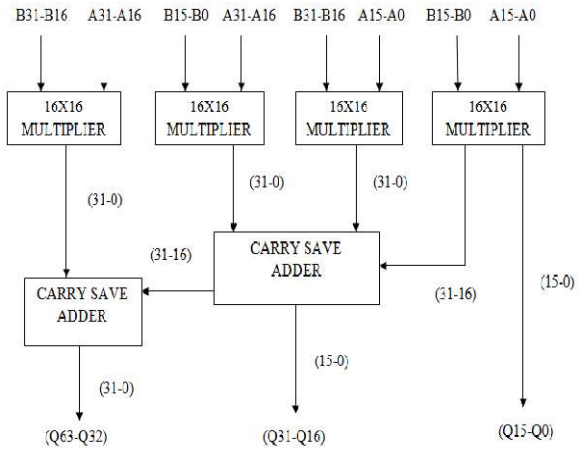

Fig (e): Implementation of 32X32 bit religious text multiplier factor RESULT → (Q63-Q32) & (Q31-Q16) & (Q16-Q0)

VI. TESTS AND RESULTS

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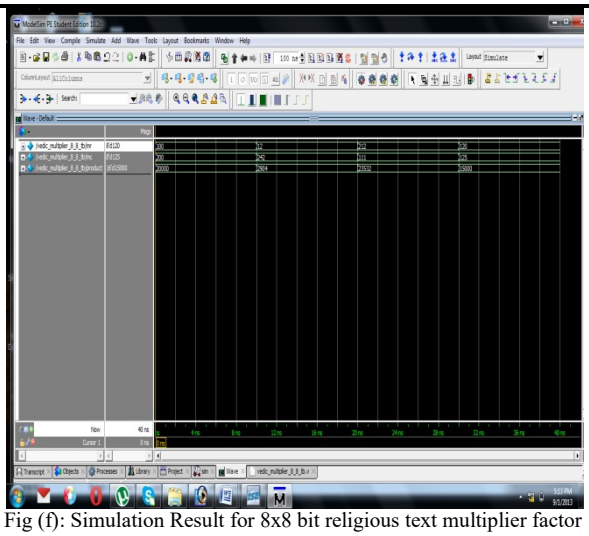

Fig (f): Simulation Result for 8x8 bit religious text multiplier factor

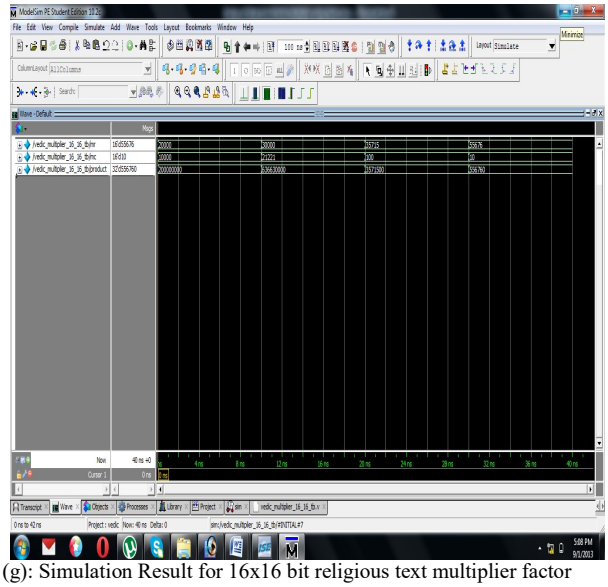

Fig (g): Simulation Result for 16x16 bit religious text multiplier factor

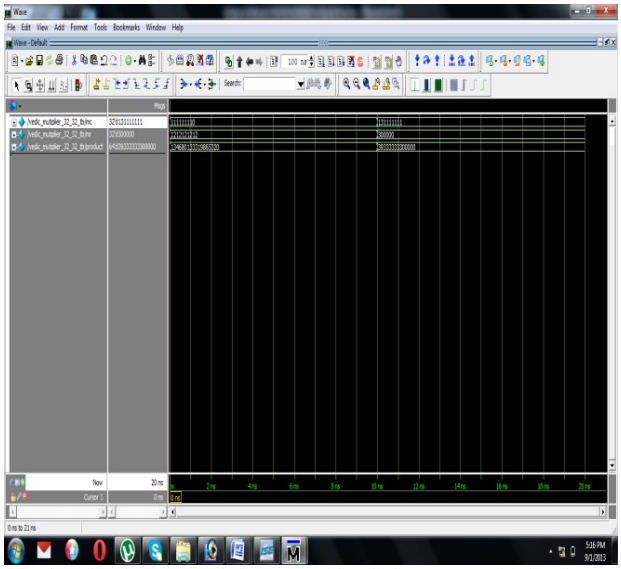

Fig (h): Simulation Result for 32x32 bit religious text multiplier factor

Synthesis Results

Selected Device: xc6vlx75t-3ff484
Number of Slice LUT's: 2387 out of 46560 1/3
Number of Slice Flip Flops: zero out of 2387 1/3
Number used as logic: 2387
Number of IOs: 128
Number of secured IOBs: 128 out of 240 fifty three
Output on digital display Screen = A0A0A09F5F5F5F60 (In hexa).

Table 1: Delay Comparison of religious text multiplier factor and traditional multiplier factor

Name Of The Multiplier	Vertex6		Vertex 6 low power	
	16x16	32x32	16x16	32x32
Vedic Multiplier	14.633ns	18.958ns	17.766ns	22.8137ns
Conventional Multiplier	26.076ns	28.533ns	31.951ns	34.616ns

VII. CONCLUSION

The styles of 32x32 bits religious text multiplier factor are enforced on Vertex6 xc6vlx75t-3ff484. the planning is predicated on religious text technique of multiplication [3]. The worst case propagation delay within the Optimized religious text multiplier factor case is eighteen.958ns and traditional multiplier factor is twenty eight.076ns. it's thus seen that the religious text multipliers ar a lot of quicker than the standard multipliers. this provides United States technique for stratified multiplier factor style. that the style complexness gets reduced for inputs of huge no of bits and modularity gets multiplied. Urdhva tiryakbhyam, Nikhilam and Anurupye sutras ar such algorithms which may scale back the delay, power and hardware necessities for multiplication of numbers. FPGA implementation of this multiplier factor shows that hardware realization of the religious text arithmetic algorithms is well potential. The high speed multiplier factor algorithmic rule exhibits improved potency in terms of speed.

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