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Optimized Architecture of Two-Stage Operational Trans-Conductance Amplifier (OTA) For Improved A_V, UGB, GM and PM

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Abstract: **Operational trans-conductance amplifier (OTA) is one of the most significant building blocks in integrated discrete-time filters used in analog to digital converter (ADC) for Sigma-delta converter [8-9]. In this paper a novel design approach is used to design a modified Two-Stage CMOS OTA using Cadence 180nm technology. A basic circuit for Two-Stage topology is used to improve the design parameters like gain, unity gain bandwidth product, gain and phase margins [1-3]. In this paper, a typical design procedure was carried to maintain the stability of the circuit. Simulation results confirm the proposed OTA circuit.**

Index Terms: **Two-Stage CMOS OTA, Op-Amp, Gain, Bandwidth.**

I. INTRODUCTION

For many circuit designs, single stage amplifiers are incapable to achieve sufficient gain, bandwidth and improper input-output impedance matching consideration. Due to this reason cascaded single stage amplifiers are used, known as multi stage amplifiers to achieve such limitations [4-5]. One of the limitations of amplifier design is in achieving low noise along with high gain, which cannot be executed in single stage amplification.

A two stage amplifier is used for optimizing the noise of first stage and working with the second stage for highest gain [5]. Amplifiers that are used for optimization or implementation of input offset correction are referred to as instrumentation amplifiers (INA) [3]. An INA differs from an operational amplifier (Op-Amp) with regard to the lack of feedback loop. Op-Amps can be configured to perform functions like inverting amplifier, non-inverting amplifier and differential amplifier, voltage follower and many more. In all these cases a feedback loop from the output to the input of Op-Amp is provided, and that feedback loop refers to the type of the function or case of Op-Amp. In electronic amplifiers, an Op-amp is referred to as voltage controlled voltage source (VCVS) device, which delivers an output voltage, i.e. it works in voltage mode [1-2].

On the other hand, an operational trans-conductance amplifier is referred to voltage controlled current source (VCCS) device, which delivers an output current, that is it works in current mode. Hence a noticeable difference between Op-Amp and OTA is that, Op-Amp is an amplifier which has high input impedance and low output impedance whereas an OTA is the one which has high input impedance and high output impedance [10].

These impedance considerations for both designs are consistent with the analog design, according to which, (i) When the input signal of interest is voltage, high impedance in required as it minimizes attenuation, (ii) When the output signal of interest is voltage, low impedance is required as its value will not vary a lot with load and (iii) When the output signal of interest is current, high impedance is required as its value will not vary a lot with load.

Another noticeable difference between them is that Op-Amp architecture consists of an output buffer stage whereas OTA architecture doesn't require it [6]. A buffer amplifier stage is used for matching considerations. Hence a buffer stage is only used in Op-Amps as it finds its space to fit in the design due to unmatched impedances [7]. A basic schematic of OTA and Op-Amp are shown below in Fig1 (a) & (b).

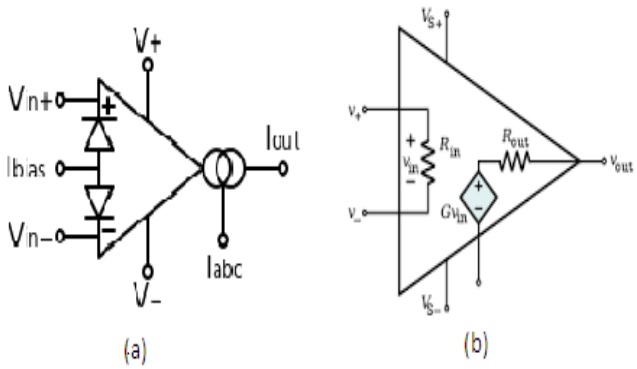

Fig1: Schematic of (a) OTA & (b) Op-Amp

The architectures of both OTA and Op-Amp are similar except for a buffer stage. Based on the applications various topologies are defined namely telescopic, folded cascade and two stage amplifiers [7]. As discussed earlier, when there is need for high gain along with low noise a two stage amplifier is taken into consideration [5].

II. DESIGN CONSIDERATIONS

A basic circuit of complementary metal oxide semiconductor (CMOS) OTA using the two stage topology is shown in Fig2 [5]. The circuit basically consists of

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differential gain stage and second gain stage. The differential gain stage consists of transistors Q1, Q2, Q3 and Q4. A driver stage is being served by using the gate of Q1 (inverting input) and the gate of Q2 (non-inverting input). The trans conductance (g_m) of this stage solely depends on Q1 or Q2. Whereas Q3 and Q4 serves as current mirrors formed by the active load transistors for this stage.

The second stage is a current sink load inverter consisting of Q6 and Q7 transistors, which provides additional gain in the amplifier [6]. This stage takes the output from the drain of Q4 and amplifies through Q6 which is in the standard common source configuration with a current sink load Q7. The biasing is achieved with a current mirror circuit consisting of Q5 and Q8 along with current source I_{Bias}. MOS Transistor Q5 and Q7 sink a small amount of current based on their gate voltage, driven by the drain voltage of Q8.

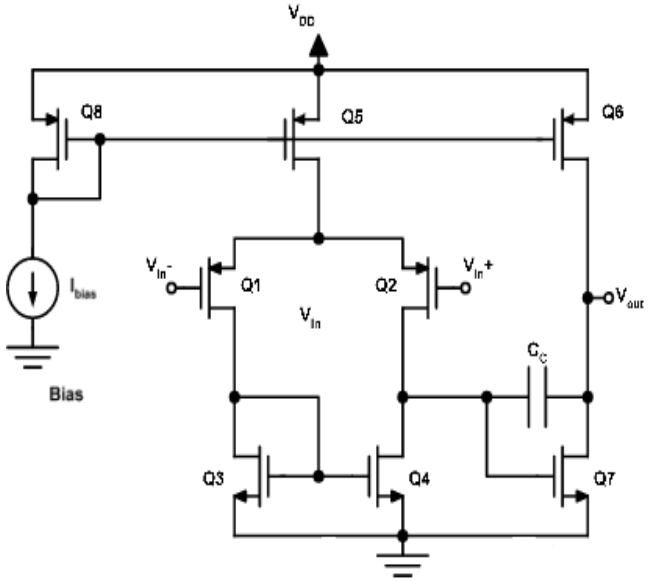

Fig2: Basic two stage CMOS OTA

In this paper, a modified two stage OTA circuit is being designed as shown in Fig3 in order to improve the design parameters [7]. The circuit shown is similar to the basic two stage OTA circuit with regard to the differential stage and second gain stage. The need of such modified circuit occurs in low voltage design wherein current source should be in coordinance with the requirement of low input and output voltages[1-3]. For such designs a cascode current mirror is required in the biasing circuit, unlike the current mirror achieved in Fig2 using transistors Q5 and Q8. The output impedance and accuracy plays an important role in the performance of current mirrors [4].

A high output impedance is thus acheived with cascode current mirror formed using the transistors Q9, Q10, Q11 and Q12 of Fig3 [6]. Each cascode circuit increases the output impedance by a factor of ($1 + g_m r_{out}$), where g_m is the transconductance and r_{out} is the output resistance of Q11 and Q12.

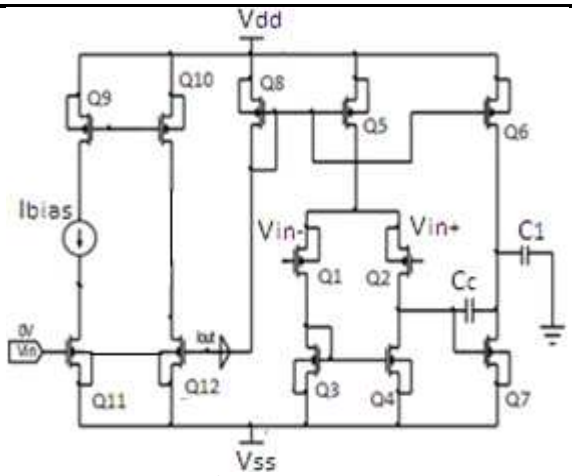

Fig3: Modified Two-Stage CMOS OTA

Table1: Design parameters of Modified Two-Stage OTA

MOS Device	Parameters	
	W(µm)	L(µm)
Q1, Q2	3	1
Q3, Q11	4.5	1
Q4	14	1
Q5, Q8, Q9	15	1
Q6	94	1
Q7	6	1
Q10	2	1
Q12	2	1
V_{dd}	3.5V	
V_{ss}	-3.5V	
C_c	4pF	
C_1	10pF	

The design parameters of Fig3 are illustrated in Table1 for acheiving a current source of 35µA. This circuit thus provides a high output impedance along with a low systematic error [11].

IV. DESIGN PROCEDURE

The design procedure assumes that the DC gain (A_v), unity-gain bandwidth (GB), Input common-mode range [V_{in} (min) & V_{in} (max)], Load capacitance (C_L), slew rate (SR), Settling Time (T_s), Output voltage swing [V_{out} (max) & V_{out} (min)] and Power dissipation (P_{diss}) are given [3,10].

1. Based on Table1, smallest device length that gives good matching for current mirrors has been chosen.
2. From the desired phase margin of 60^0, the minimum value for C_c is chosen. This assumes that $C_c > 0.22\ C_L$
3. The minimum value for the tail current (I_5) is determined. $I_5 = SR.C_C$, I_5 nearly equal to $\frac{10(V_{DD}+|V_{SS}|)}{2T_S}$
4. Design for S_3 from the maximum input voltage specification.

$$S_3 = \frac{2I_5}{K_3^1 V_{DD} - V_{in(max)} - \left[V_{T3(max)} + V_{T1(min)}\right]^2} \geq 1$$

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5. The pole and zero due to C_{gs3} and C_{gs4} $(=0.67W_{3L3}C_{ox})$ will not be dominant by assuming pole p_3 to be greater than 10GB. $\frac{g_{m3}}{2C_{gs3}} > 10GB$

6. Design for S_1 (S_2) to achieve desired GB.

$$g_{m1} = GB.C_c \geq S_1 = S_2 = \frac{g_{m2}}{K_2^1 I_5}$$

7. Design for S_5 from the minimum input voltage. First we have calculated $V_{DS5(sat)}$ and then we have find S_5.

$$V_{DS5\,(sat)} = V_{in\,(min)} - V_{SS} - \left(\frac{I_5}{\beta_1}\right)^{\frac{1}{2}} - V_{T1\,(max)} \geq 100mV$$

$$S_5 = \frac{2I_5}{K_5^1 [V_{DD\,(sat)}]^2}$$

8. Find S_6 and I_6 by letting the second pole (p_2) be equal to 2.2 times GB.

$$g_{m6} = 2.2\, g_{m2} \left(\frac{C_L}{C_c}\right)$$

Let $V_{SG4} = V_{SG6}$, which gives $S_6 = S_4 \left(\frac{g_{m6}}{g_{m4}}\right)$

9. Alternately, I_6 can be calculated by solving for S_6 using $S_6 = \frac{g_{m6}}{K_6^1 V_{DS6\,(sat)}}$

10. Design S_7 to achieve the desired current ratios between I_5 and I_6.

$$S_7 = \left(\frac{I_6}{I_5}\right) S_6$$

11. Check gain and power dissipation specifications.
12. By simulating the circuit we have seen that all the specifications are met.

V. SIMULATION RESULTS

In this paper, simulation was carried out on Cadence tool for 180nm technology [5].

The device parameters were designed using the design procedure and values from Table1. Transient response and AC response were studied using the tool and it was observed that the modified circuit when compared to the basic circuit gives a better gain and phase margins at microwave frequencies as shown in the comparative results in Table2.

Table2: Comparative results

Parameter	Basic Two-Stage OTA	Modified Two-Stage OTA
Technology	180nm	180nm
A_v	42dB	48dB
UGB	20MHz	40MHz
GM	15dB	46Db
PM	49º	89.8º
SR	0.13V/µs	0.10V/µs
f_c	82KHz	85KHz
V_{out}	-1.4 to 1.2V	-1.3 to 1.3V
T_s	17ns	15.6ns

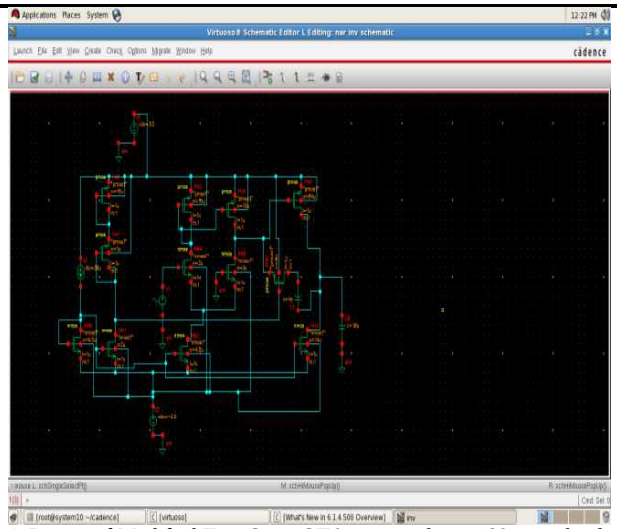

Fig4: Design of Modified Two-Stage OTA using cadence 180nm technology.

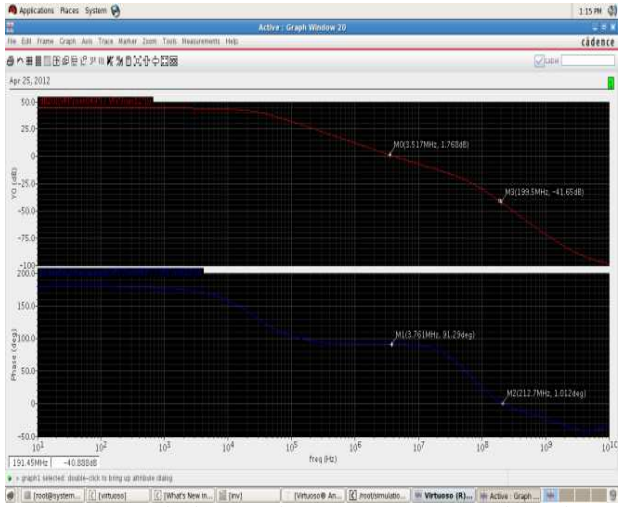

Fig5: Simulated transfer functions for magnitude and phase of Modified Two-Stage OTA using cadence 180nm technology.

V. CONCLUSION

Design of OTA plays a vital role in integrated discrete-time filters used for design of Sigma-Delta converter [8-9]. This work presents a novel design method of Two-Stage CMOS OTA which has been designed and compared with Basic Two-Stage OTA. Behavioral simulation indicated that phase margin is 89.8° to ensure a good stability, gain of 48 dB for ±3.5V without using a gain boosting technique, and Unity gain bandwidth (UGB) of 40 MHz is sufficient to design the ADC converter [8]. The applied technique leads to a significant preservation in unity gain bandwidth product (GBW), gain (A_v), slew rate (SR), and decrease power consumption.

The design technique proposed in this paper combines better performance with simplicity of design and suitability for high frequency operation with few modifications on conventional two-stage CMOS OTA and at low power consumption.

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