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A Review on Multiplier Designing and Optimization

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Abstract— The evolution of digital systems, have brought out new challenges in VLSI designing. Past devices were developed with the processing of input data for arithmetic and logical units to perform an operation. With the increase in integration density and demand for higher services, new processing units have evolved, which are much compact and very fast in operation. To cope with these demands, new operational units are developed. Among all arithmetic operational units, Multiplier logic is observed to be a core part to perform a numerical task. However, multipliers are observed to be high resource consuming and iterative in nature which minimizes the operational efficiency of the processing unit. This paper, reviews on the development of different multiplier designing approaches and their applications in processing level usage.

Index term: Multiplier Design, optimization, applications, VLSI, processing unit.

I. INTRODUCTION

To achieve the objective of increasing demand of high level services on compact devices, new devices were developed and, are in further development to meet the required demand. The raise in these demand has lead to developing of high processing units, performing arithmetic and logic operation at a very high speed to cope the processing demand. As new advanced interfacing units were developed, the processing need to be synchronized to give better operational efficiency. In the design of processing unit, the core processing block operating on input data is the arithmetic and logical unit (ALU). These units are responsible for performing all type of arithmetic and logical instructions, on the input data and provide the derived results. In this ALU unit, the constituent operations are arithmetic addition, subtraction, division and multiplication. The adder and sub tractor unit perform the addition and subtraction operation, whereas a shifter and adder realizes a multiplier unit. Among these operational units, multiplier units are observed to be recurrent processing and requires large resources for temporary storage and addition process. This large demand of resource results in higher area coverage and power dissipation. This effect in operation efficiency of the processing unit. To overcome this issue in multiplier designing, various past approaches were developed. This paper, outlines these developments and there limitation to design a multiplier unit. To present the review of these developments, this paper is presented in 5 sections. Where, section 2 outlines the approach of multiplier design and their optimization process. The basic constituting element of adder and shifter operations were optimized to achieve a efficient operation of a multiplier design. In section 3 the applications and limitation of the suggested multiplier unit is suggested. The conclusion derived from the made review is outlined in section 4.

II. MODELING OF MULTIPLIER UNIT

The use of digital processing has become widespread, and it provides enormous advantage in various real time applications. High frequency and increasing design complexity are stretching the limits of design tools and methodologies. Recent advances in silicon technology have made it possible to design with significantly larger gate densities and higher clock frequencies. Design engineers have used these advances to integrate more complex functionality into their system-on-chip (SoC) designs. In the digital processing of real time applications, Arithmetic operations such as addition, subtraction, multiplication and division are widely used and play an important role in various digital systems such as digital signal processor (DSP) architecture, microprocessor and microcontroller and data process unit [1]. Basically the given values are processed using mathematical operators. Among different operators multiplier unit is redundantly been used in almost all mathematical operations. This operator has its highest significance in all the real time processing units. The highest degree of usage of a multiplier unit, in real time application, make this unit a very important unit for optimization and performance enhancement. The basic principle used for multiplication is to evaluate partial products and accumulation of shifted partial products. In order to perform this operation number of successive addition operation is required. A basic operation of multiplication operation is shown in figure 1.

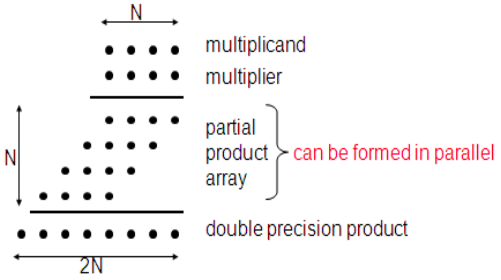

Figure 1: A N – bit multiplication operation [18,53]

Therefore one of the major components required to design a multiplier is Adder. Adders can be Ripple Carry, Carry Look

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Ahead, Carry Select, Carry Skip and Carry Save [2,3,4]. Several researchers had addressed the adder performance issues and others did the same with regard to the multiplier performance. Sertbas and Özbey worked on the performance analysis of classified binary adder architectures. They compared the ripple adder, carry-look-ahead adder, carry select adder and the conditional sum adder. They used VHDL implementation for their designs and comparison studies. Their work included the unit-gate models for area and delay [5]. A full precision bit-serial multiplier was introduced by Strader et al [6] for unsigned numbers. A full-precision scheme for 2's complement numbers has been presented in [7]. This multiplier for n-bit operands requires 2n clocks and 2n number of five-input adder modules. A serial multiplier and a squarer with no latency cycles are presented in [8] and algorithms for serial squarer's and serial/serial multipliers were derived in [9]. The signed multiplication technique was proposed which is applicable for both the signs [10]. This is a technique where binary numbers of both the sign can be multiplied by a uniform process. Multiplication involves 2 basic operations: the generation of the partial product and their accumulation. Baugh-Wooley Multiplier is used for both unsigned and signed number multiplication [11], [12]. Serial accumulation of unsigned binary numbers by high speed 1's counters is proposed in [13]. Multiplication process consists of three stages of operation, the generation of partial products (PPs), the reduction of PPs and the final carry-propagation addition [14]. Unlike the conventional CSAS architecture, the critical path is found only along the AND gates [15] as shown in figure 2.

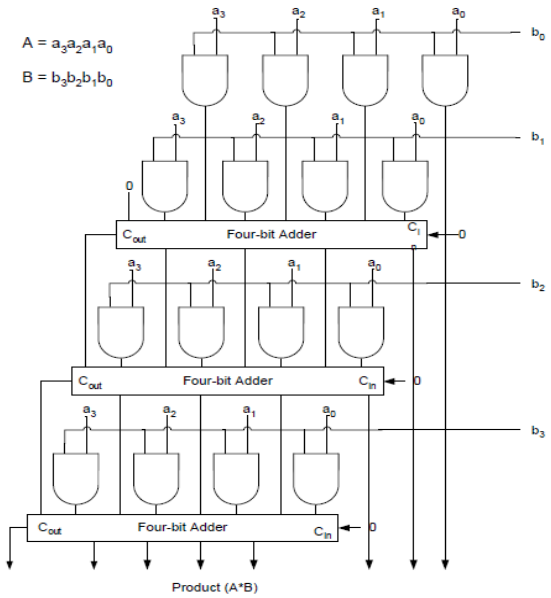

Figure 2: Basic multiplier unit using CSAS [18,53]

The rows of the partial product can be generated in n clock cycles instead of 2n clock cycles and hence delay is reduced. Column compression technique is used for reducing the height of the partial product tree height. Thus, the numbers of computational cycles are reduced. Moreover, the counters change states only when input is '1', which leads to low switching power [16,17]. Adder is one of the most important components of a CPU (Central Processing Unit). Fast adders are necessary in ALUs, for computing memory addresses. Full-adders are important components in other applications such as digital signal processors (DSP) architectures [18,19] and microprocessors. Kogge-stone adder [20] is called as parallel prefix adder [21]. Figure 3 illustrates the operation of a Kogge-stone multiplier unit.

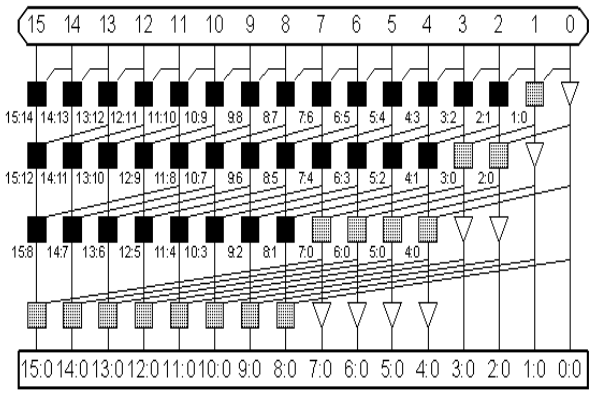

Figure 3: Kogge-stone multiplier architecture [18,53]

It is the common design for high-performance adders in industry. It is considered as the fastest adder as the computation time taken by this adder is O (log n) time [22].The logic-level implementation of the basic cells used in parallel-prefix adders is described in [23]. The basic structure of 8-bit radix-2 Kogge-Stone adder (KSA) described, operates on the principle of block propagate (p) and block generate (g).Adder is one of the most important components of a CPU (Central Processing Unit). A number of fast adders like carry-skip adder, carry-select adder and carry look-ahead adders have been proposed in the past [24-25]. Optimization of adders can be done at logic-level or circuit level. Logic-level optimization involves rearranging the Boolean equations so that a faster or smaller even less power consumption circuit is obtained. Several full adder logic cells are compared and discussed in [26].

III. APPLICATIONS AND LIMITATION

With the explosive growth of VLSI system and portable devices, the power reduction of integrated circuits has become a major problem. In applications, such as communication system, cellular phone, camcorders and portable storage devices, low power dissipation, hence longer battery lifetime, is a must. To achieve a long life operation of the portable device it is required to have a design system developed with faster operation and low power consumption. As most of the digital processing units are executed with mathematical operations, where a multiplier unit is dominantly been used, it is required to optimize a multiplier unit for overall system performance. Towards optimization of power consumption and speed improvement in [27] a digital level modeling of multiplier unit is proposed. The suggested parallel decimal multipliers are developed using VHDL definitions [28,29],

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and the power optimization [30] is observed to be evaluated for the seven mode of designing approaches in multiplier unit. Here, the design unit is developed in top down approach with delay and area coverage under consideration. The approach defines a relative energy consumption wrt. delay minimization in radix based multiplication operation [31,32]. Wherein delay is lower in radix operation, power consumption is observed to be high due to recurrent design approach. It is hence required to develop a equilibrium modeling in such design using delay-power optimization. Towards the objective of achieving higher performance with low power consumption in [33,34,35] bit level optimization is suggested. The coding efficiency in such coding is suggested via high level bit processing [36], suggested in ternary level operations. In the ternary level operation, the given bits are represented in 3 levels rather to 2 level representations as in binary mode. Due to 3 level representations, the processing speed of the system is observed to be higher, but the system overhead and area constraint are higher for such design. In recent approaches toward multiplier optimization, Vedic approach [37] of design modeling is emerging. This mode of design uses the concept of vedic Maths to realize high level mathematical operation in a simpler modeling. Towards this approach in [38,39,40,41] a high speed floating point operator using vedic approach is suggested. The suggested multiplier unit, optimizes the usage based on successive adder and or units to achieve the results. In this approach, the speed of operation is observed to be higher, however, temporary buffering of the results bits are an overhead to this coding approach. There is a large register usage in such coding. The multiplier compiler design defined in [42] and [43] generate parameterizable layout for MOS technology, thus making them suitable for various high speed, low power, and compact VLSI implementations. However area and speed are two important conflicting constraints. For real-time signal processing, a high speed and throughput Multipliers-Accumulator (MAC) is always a key to achieve high performance in the digital signal processing system. The main consideration of MAC design is to enhance its speeds. That high speed is achieved through this well-known Wallace tree multiplier [45,46]. Wallace introduced parallel multiplier architecture [47] to achieve high speed. A Basic architecture is shown in figure 4.

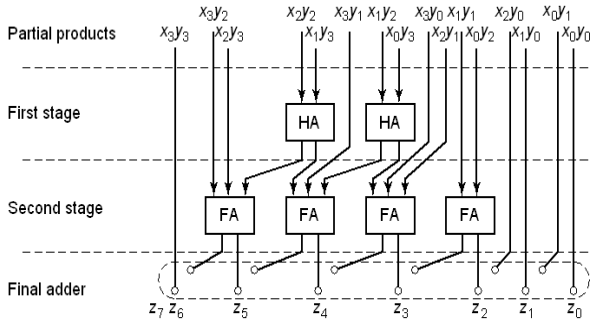

Figure 4: Wallace tree approach to Multiplier [18,53]

Wallace Tree algorithm can be used to reduce the number of sequential adding stages. The advantage of high speed becomes an enhanced feature for multipliers having operand of greater than 16 bits. The Wallace tree was being constructed using carry save adder to reduce an N row bit product matrix to an equivalent two row matrix that is then fed into carry propagating adder to sum up those rows of bits and to produce the product. The carry save adders are those conventional full adders [48] in which carries are not connected and three bits of inputs are taken in and two bits are given as output. The Wallace Tree multiplier has an irregular structure. Many different adder tree structures have been used to reduce the computation time of the multipliers. The main disadvantage of Wallace tree multipliers is its irregular structure, making layout difficult and all adder blocks are active regardless of multiplicand size. More area on the wafer and needs greater cell interconnection wiring. Since an interconnection plays an important role in IC technologies this factor makes Wallace tree inappropriate for certain circuits. The main advantage of this multiplier is its Logarithmic circuit delay [49]. In many FPGAs, Wallace trees do not provide any advantage over ripple adder trees. Due to irregular routing, they may actually be slower and may certainly more difficult to route. Adder structure used in this will increases for increased bit multiplication. To achieve high-speed multiplication, algorithms using parallel counters like modified Booth algorithm [51] has been proposed as shown in figure 5.

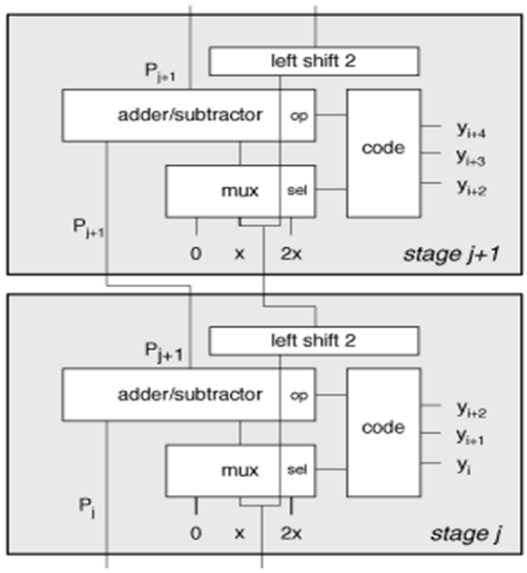

Figure 5: Booth Multiplier unit [18,53]

This type of fast multiplier operates much faster than an array multiplier for longer operands because it's time to compute is proportional to the logarithm of the word length of operands. By recoding the numbers that are to be multiplied, Modified Booth multiplier [50] allows for smaller, faster multiplication circuits. The number of partial products is reduced to half, by using the technique of Booth recoding. The advantage of this method is making the number of partial products into half of the multiplier term size by grouping. The main disadvantage of the modified booth multiplier is its complexity of the circuit to produce partial product. For the past few years, different optimizations have been applied in the architecture in order to

minimize the dynamic power dissipation in arithmetic circuits, and especially in digital multipliers. In this Mixed Style Multiplier [51], there are two parts of multipliers. One is array part and the other one is a tree part multiplier. The array multipliers are chosen for this bypassing technique since it has a regular interconnection which helps to skip unwanted blocks. The array multipliers have linear delay circuit. The second part is a tree part multiplier which has the advantage of logarithmic circuit delay and considered to produce results in faster way.

IV. CONCLUSION

This paper outlines an extensive review on the developments made in the area of multiplier design. The Design approaches developed for fixed and float data type multipliers are presented. The applications of such multiplying unit in the real time usage is presented. The optimization multiplier design using resources utilization and scheduling approaches are presented. The resource optimization problem based on power consumption and hardware efficiency is observed. The upcoming approach of Vedic algorithm in usage of arithmetic operation and its usage in multiplier design is presented. The limitation in regards to these conventional design approach is addressed.

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