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Design and Implementation of a 4:2 Compressor Design with New XOR/XNOR Modules using Backend Tools

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Abstract: **- In this paper realization of a low-power high speed 4:2 compressor circuit is proposed for fast digital arithmetic integrated circuits. Most of the VLSI circuits used adders as a crucial portion, since they form the base element of all arithmetic functions. Increasing demand for portable equipments requires area and power efficient VLSI circuits. This project presents 4:2 compressor using different full adder designs. The aim of this project is to reduce the power consumption of 4:2 compressors without compromising the speed and performance. Full adder is fundamental unit in various circuits, especially, in performing arithmetic operations such as compressors, comparators, parity checkers, multipliers etc. It is the nucleus of many other useful operations such as subtraction, multiplication, division, exponentiation, address calculation and can significantly influence the overall achievable performances of the system. Compressors, in its several variants, are logic circuits which are capable of adding more than 3 bits at a time as opposed to a full adder and capable of performing this with a lesser gate count and higher speed in comparison with an equivalent full adder circuit. A compressor adder is a logical circuit which is used to improve the computational speed of the addition of 4 or more bits at a time. Compressors can efficiently replace the combination of several half adders and full adders, thereby enabling high speed performance of the processor which incorporates the same. The designed compressor has been verified by using the TANNER EDA. Layouts are designed using BACKEND Tools. Existed compressor design consists of more transistors. The designing could be little complex. Power consumption could be high. In this proposed system 4:2 compressor has been designed and implemented, with the new XOR-XNOR module with eight transistors and transmission gate 2:1 multiplexer without the output buffers. This multiplexer design is faster and dissipates low power than the standard CMOS design. For Microchip manufacturing in different level of circuits we are using compressor designs to reduce the size of chips to implant easy and for easy portable. For power management of different circuits at different level of complex circuits we are using this compressor designs.**

Keywords: 4:2 compressors, full adder, XOR-XNOR module, Transmission gate with 2:1 multiplexer, TANNER EDA and Power management.

1. INTRODUCTION

The main object of our project is to "Design and Implementation of a 4:2 Compressor Design with New XOR/XNOR Modules Using Backend Tools"**.** A low-power high speed 4:2 compressor circuit is proposed for fast digital arithmetic integrated circuits. This has been widely employed for multiplier realizations. Based on a new exclusive OR (XOR) and exclusive NOR (XNOR) module, a 4:2 compressor circuit has been designed. Proposed circuit shows power consumption variation. This 4:2 compressor circuit have been compared with earlier reported circuits and proposed circuit is proven to have the minimum power consumption and the lowest delay. In proposed system we overcome disadvantage of existing system like area, delay, Power dissipation, performance of design and complexity of circuit.

1.1 Problem Statement:

The circuit performs successfully at low supply voltages but this comes at the expense of increased area and number of transistors. Another disadvantage of the circuit is that each of the inputs drives four gates instead of two gates doubling the input load. This will cause slow response when this circuit is cascaded. In previous projects compressor designed using static cmos, cmos logic design styles which includes pass transistor design, dual pass transistor design and complementary design, standard mux designs having the more number of transistors. The designing of the compressor is also little complex and hard to design. In existing system Power consumption could be high with low performance. To overcome these problems in existing system we have designed proposed design. This improves all these aspects.

2. LITERATURE SURVEY

2.1 Overview

Additionally, the asymmetric input logic levels make PMOS circuits susceptible to noise. Though initially easier to manufacture, PMOS logic was later supplanted by NMOS logic because NMOS is faster than PMOS. Modern Designs use CMOS, which uses both PMOS and NMOS transistors together. Static CMOS logic leverages the advantages of both by using NMOS and PMOS together in the wafer. The worst problem is that a DC current flows through a PMOS logic gate when the PUN is active that is whenever the output is high. This leads to static power dissipation even when the circuit sits idle.

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Additionally, just like in DTL, TTL and ECL etc., the asymmetric input logic levels make NMOS circuits somewhat susceptible to noise. These disadvantages are why the CMOS logic now has supplanted most of these types in most high-speed digital circuits such as microprocessors (despite the fact that CMOS was originally very slow).Also, NMOS circuits are slow to transition from low to high.

2.2 CMOS Logic Design Styles

Complementary Metal Oxide Semiconductor is a widely used semiconductor technology used in the transistors. It uses both NMOS (negative polarity) and PMOS (positive polarity) circuits, but only one of the circuit types is on at any given time, due to which it requires less power than chips using just one type of transistor. Since it requires very less power, it is ideal for use in Personal Computers, microprocessors, microcontrollers, and other digital logic circuits. CMOS is sometimes referred to as complementary-symmetry metal–oxide–semiconductor (COS-MOS). Here the words "complementary-symmetry" refers to the fact that CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor.

2.3 Impact of Logic Style

The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. The circuit delay is determined by the number of inversion levels, the number of transistors in series, transistor sizes (i.e., channel widths), and intra- and inter-cell wiring capacitances. Circuit size depends on the number of transistors and their sizes and on the wiring complexity. Power dissipation is determined by the switching activity and the node capacitances (made up of gate, diffusion, and wire capacitances), the latter of which in turn is a function of the same parameters that also control circuit size. Finally, the wiring complexity is determined by the number of connections and their lengths and by whether single-rail or dual-rail logic is used. All these characteristics may vary considerably from one logic style to another and thus make the proper choice of logic style crucial for circuit performance. As far as cell-based design techniques (e.g., standard-cells) and logic synthesis are concerned, ease-of-use and generality of logic gates is of importance as well. Robustness1 with respect to voltage and transistor scaling as well as varying process and working conditions, and compatibility with surrounding circuitries are important aspects influenced by the implemented logic style.

2.4 Logic Style Requirements for Low Power

$$P_{dyn} = V_{dd}^2 \cdot f_{clk} \cdot \sum_n \alpha_n \cdot c_n + V_{dd} \cdot \sum_n i_{sc_n}$$

According to the formula dynamic power dissipation of a digital CMOS circuit depends on the supply voltage, the clock frequency , the node switching activities the node capacitances, the node short circuit currents and the number of nodes. A reduction of each of these parameters results in a reduction of dissipated power. However, clock frequency reduction is only feasible at the architecture level, whereas at the circuit level frequency is usually regarded as constant in order to fulfill some given throughput requirement. All the other parameters are influenced to some degree by the logic style applied. Thus, some general logic style requirements for low-power circuit implementation can be stated at this point.

3. IMPLEMENTATION

A new architecture is presented. In this architecture the emphasis lay on the use of multiplexers instead of XOR gates. This is because the use of multiplexers improves the speed when placed in the critical path. For the XOR-XNOR module, this work uses the traditional CMOS logic style and for the MUX module they use a combination of a traditional CMOS logic style with a transmission gate logic style that is only used in the internal paths of the adder due to the limited driving capability.

Proposed MUX Block Representation:

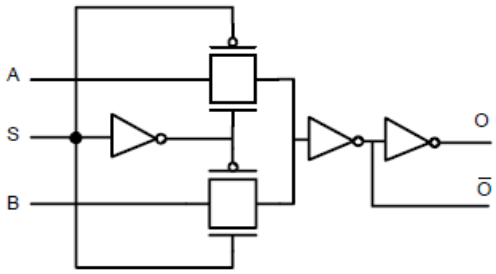

Fig 3.1 Multiplexer (MUX) implemented with transmission Gates.

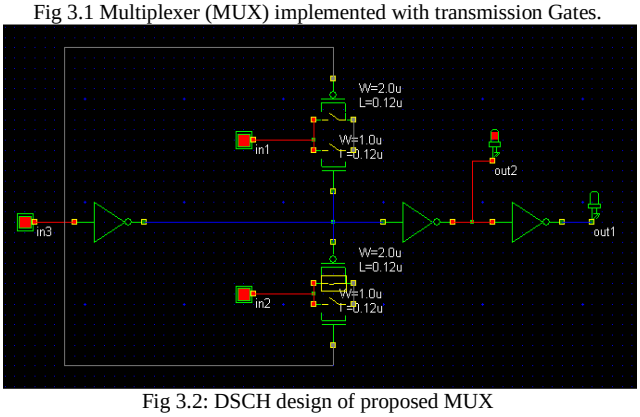

Fig 3.2: DSCH design of proposed MUX

Proposed MUX Waveforms:

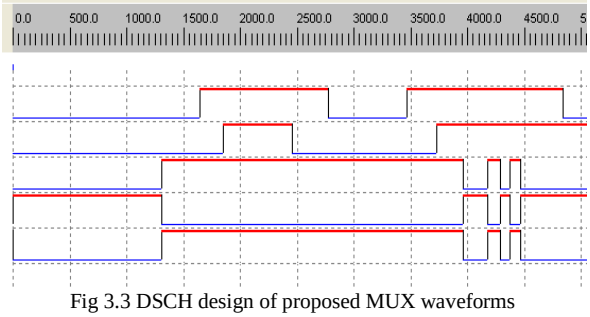

Fig 3.3 DSCH design of proposed MUX waveforms

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Proposed XOR/XNOR Design:

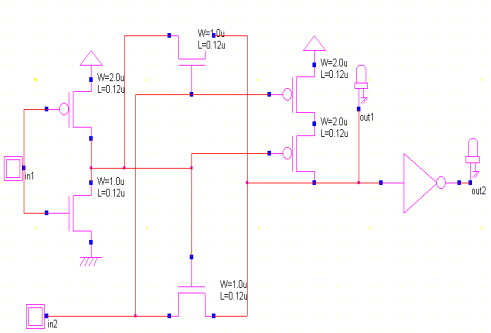

Fig 3.4 DSCH design of proposed XOR/XNOR

Proposed XOR/XNOR Design Waveforms:

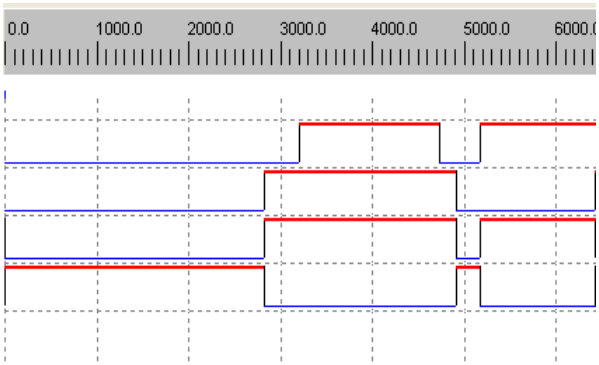

Fig 3.5 DSCH design of proposed XOR/XNOR waveforms

4. TANNER SOFTWARE

Today's semiconductors and electronic systems are complex that designing them would be impossible without electronic design automation (EDA). This primer provides a comprehensive overview of the electronic design process, and then describes how design teams use Cadence tools to create the best possible design in the least amount of the time.

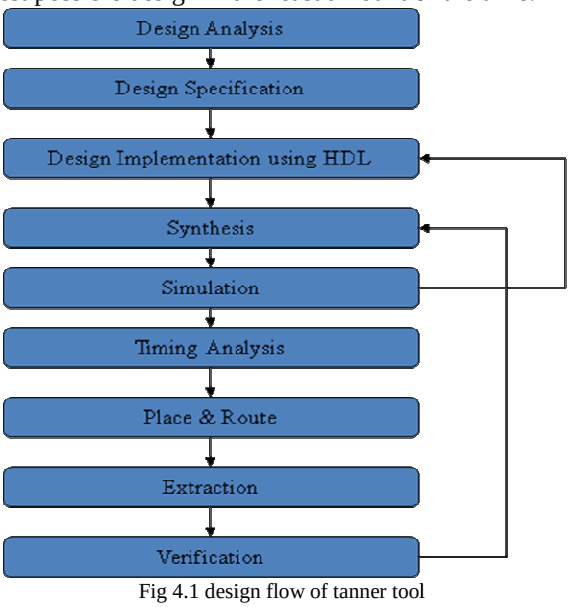

Fig 4.1 design flow of tanner tool

5. SIMULATION AND RESULTS

Proposed 4:2 Compressor Schematic Design:

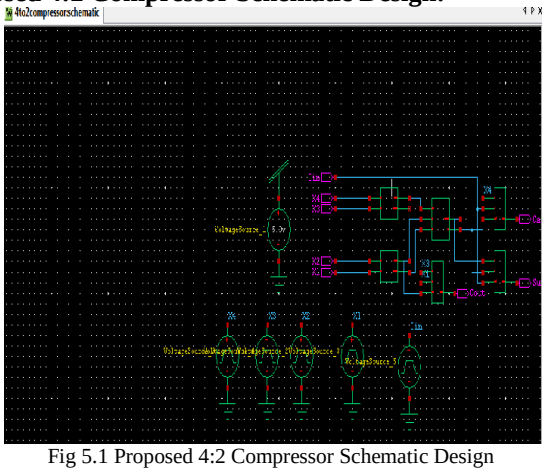

Fig 5.1 Proposed 4:2 Compressor Schematic Design

Proposed 4:2 Compressor Simulations:

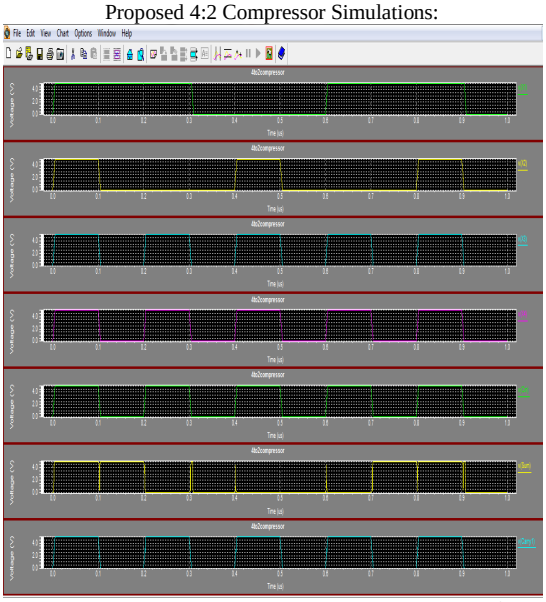

Fig 5.2 Proposed 4:2 Compressor Schematic Design waveforms

Proposed 4:2 Compressor Design Layout:

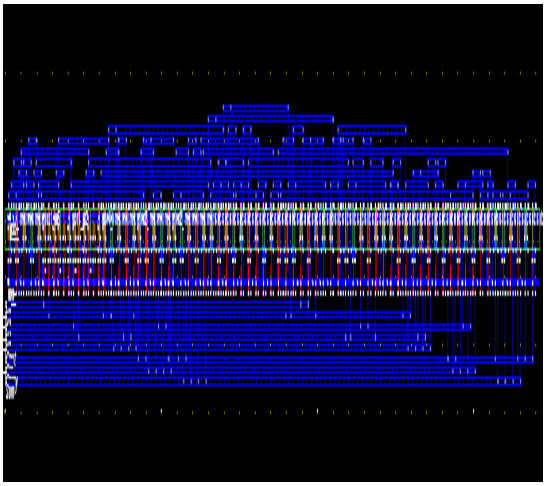

Fig 5.3 Proposed 4:2 Compressor Design Layout

Conclusion: A 4-2 compressor circuit based on a new XOR-XNOR design has been proposed which provide better performance. The proposed XOR-XNOR design shows power consumption of 1.122486e-006 pW. The proposed 4-2 compressor circuit shows power consumption of 6.064625e-006 pW. The performance of this circuit have been compared to earlier reported circuits in terms of power consumption, maximum output delay and power delay product (PDP). The proposed circuit result shows better performance than existing circuits in all aspect.

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