



# A High Performance Inverter Based Comparator Design

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**Abstract:** In high-speed high-resolution analog to digital converters, comparators have a key role in quality of performance. High power consumption and delay is one of the drawbacks of these circuits which can be reduced by using suitable architectures. Many versions of comparator are proposed to achieve desirable output in sub-micron and deep sub-micron design technologies. Back to-back inverter in the latch stage is replaced with dual-input single output differential amplifier. This topology completely removes the noise that is present in the input. The structure shows lower power dissipation and higher speed than the conventional comparators. The circuit is simulated with 0.8V DC supply voltage and 250 MHz clock frequency. The proposed circuit analyses the Inverter based differential amplifier design compared to double tail comparator, is a less delay and controls the power dissipation. Finally output results shown by using T-Spice tool in TSMC018

**Keywords** – CMOS comparator, low power, High Speed, Analog-to-Digital Converter and Tanner EDA

## 1. INTRODUCTION

The rapidly growing market of portable electronic systems such as wireless communication devices, consumer electronics or battery-powered medical devices increases the demand for developing low voltage and low-power circuit techniques and building blocks. One such application where low power, high resolution and high speed are required is analog -to-digital converters (ADCs) as a key components in mixed-signal integrated circuits. Recent ADC applications are used increasingly in digital data reading fields, such as hard disk drives, digital video discs and local area networks. High

sampling speed is required in all of these applications, best solution for high speed, low latency operations is flash architecture but performance degrades as number of comparator increases. Alternative to this folding CMOS comparator which reduces number of comparators but performance degrades due to process variation. A novel circuit for low power, low cost, high speed CMOS ADC is general successive approximation ADC is presented where comparators plays a key role.

Greatly affect the overall performance of the device. One such application where low power dissipation, low noise, high speed, less hysteresis, less Offset voltage are required is Analog to Digital converters for mobile and portable devices. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The accuracy of such comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. In the past, pre-amplifier based comparators have been used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparators is the more offset voltage. To overcome this problem, dynamic comparators are often used that make a comparison once every clock period and require much less offset voltage. However, these dynamic comparators suffer from large power dissipation compared to pre-amplifier based comparators. The main problem with all these dynamic comparators is the output signal of the latch stage is fluctuating during clock transition. This is happening due to the presence of noise in input terminals. In this paper we have designed all type of comparators.



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## Dynamic Vs. Static Logic

Static Logic always has a path from power or ground to the output

- Stable over long periods
- Simple clocking schemes
- Dynamic Logic relies on capacitance of gates or other structures to hold state
- Can be faster than static logic
- Has minimum operating frequency
- More restrictions about how/when inputs can change
- Consequence of how we implement dynamic logic

## Dynamic Logic Concepts

- All dynamic logic we'll look at is clocked
- In one phase of the clock, we'll pre charge the gate to either 0 or 1.
- In another phase, we'll evaluate whether the gate's output should stay at the pre charged value or change.

In this Dynamic comparator designs there will be two phases one was Reset phase when  $\text{Clk}=0$  and then Latch Phase when  $\text{Clk}=1$ .

## Need of this work:

Traditional operational amplifier designs most commonly use transistors in the saturation region, which generally requires at least one DC bias current. As technology size has decreased, low power, high gain amplifier design has become more challenging for designers. Since transistor threshold voltage generally doesn't decrease as fast as feature size and power supply voltage, many cascaded or folded designs are not possible with reduced voltage supply. Given that the reduction in headroom reduces the ability to cascode devices, low voltage high-gain amplifiers are commonly built by expanding outward, using two or even three cascaded amplification stages. These multi-stage cascaded designs require the designer to take extra measures to ensure amplifier stability, and, depending on the topology, can be very challenging or complex to stabilize. Most stabilization schemes require additional compensation capacitors and/or nulling resistors, which use additional silicon area, and can decrease circuit

bandwidth; however, these compensation Reduced power supply voltage and the increasing demand for low power consumption make sub-threshold operation and design a more viable alternative when a reduction in bandwidth is acceptable. Operation in the sub-threshold region causes the drain current to increase exponentially with VGS as opposed to quadratically in the saturation region.

The disadvantage with sub-threshold operation is the reduction in amplifier driving current, and the loss of ability to quickly drive large capacitive loads.

In this paper, an inverter-based operational amplifier topology and operation and design principles are discussed and evaluated. We use two previously used figures of merit to objectively compare various aspects of the different circuit topologies. We conclude that the inverter-based differential amplifier topology with current starving provides one of best circuit topologies for energy efficiency

## 2. DESIGN PROCEDURE

A high speed latched comparator using positive feedback based back to back latch stage, suitable for pipelined Analog to Digital converter, with reduced delay and high speed is proposed During the RESET PHASE, when Clk is LOW ( $\text{Clk}=0$ ), transistor NMOS\_5 is in off state and pmos transistors PMOS\_3, PMOS\_6, PMOS\_7, are in on state. Transistors NMOS\_1 and NMOS\_2 are in cutoff mode. Switch transistors PMOS\_3, PMOS\_9, PMOS\_4, and PMOS\_10 will charge the drains of transistors NMOS\_1 and NMOS\_2 and the output nodes Outp and Outn towards Vdd. During the REGENERATION PHASE, when Clk is HIGH ( $\text{Clk}=1$ ), The process starts by turning the transistor NMOS\_3 on and immediately an current 'I' starts to flow and the drain of transistor NMOS\_3 starts to discharge towards ground (Gnd). In this succession the differential input transistors NMOS\_3 and NMOS\_4 are turned on. The currents of transistors NMOS\_1 and NMOS\_2, (at the drain terminal) will start to pull the output nodes Outp and Outn towards Gnd. Due to the difference of voltages between the input signals, the current at the drain terminals of transistors NMOS\_3 and NMOS\_4 will be different. Now in the regeneration mode the

output node are discharging towards Gnd and pmos transistors PMOS\_1 and PMOS\_2 will come in saturation mode as the voltage at output nodes falls below. The design is simulated using 0.25µm CMOS Technology using Tanner EDA Tools. Proposed design exhibits reduced delay and high speed with a 5.0 V supply. This design can be used where high speed and low propagation delay are the main parameters schemes have been improving with the usage of active compensation networks.

### 3. PROPOSED DYNAMIC COMPARATOR

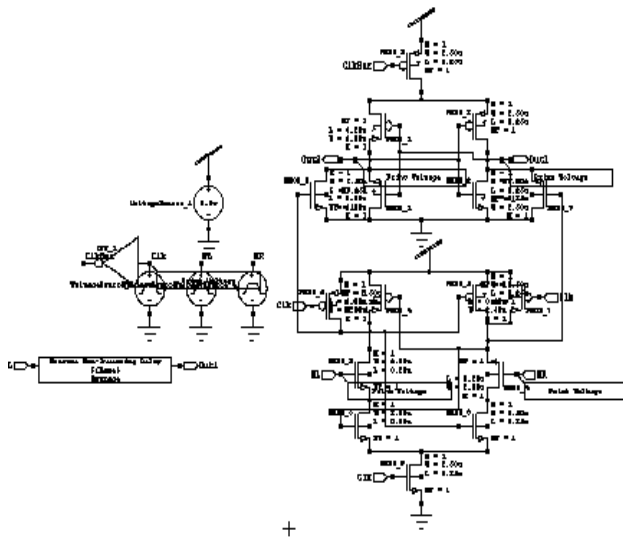


Fig.1 Final structure

The proposed comparator provides better input offset characteristic and faster operation in addition to the advantages of those comparators such as less kickback noise, reduced clock load and removal of the timing requirement between Clk and Clkb over a wide common mode and supply voltage range. The overall area is small even though number of transistors is more. It is because of widths of transistors are optimized without compromising the speed and performance of the comparator.

For its operation, during the pre-charge (or reset) phase (Clk=0V), both PMOS transistor PMOS\_6 and PMOS\_7 are turned on and they charge Di nodes' capacitance to VDD, which turn both NMOS transistor NMOS\_1 and NMOS\_2 of the inverter pair on and Di' nodes discharge to ground. Sequentially, PMOS transistor PMOS\_1, PMOS\_2, PMOS\_6

and PMOS\_7 are turned on and they make Out nodes and SW nodes to be charged to VDD while both NMOS transistors NMOS\_4 and NMOS\_3 are being off. During the evaluation (decision-making) phase (Clk=VDD), each Di node capacitance is discharged from VDD to ground in a different time rate proportionally to the magnitude of each input voltage. As a result, an input dependent differential voltage is formed between Di+ and Di- node. Once either Di+ or Di- node voltage drops down below around  $VDD - |V_{tp}|$ , the additional inverter pairs PMOS\_1/ NMOS\_1 and PMOS\_2/ NMOS\_2 invert each Di node signal into the regenerated Di' node signal. Then the regenerated and different phased Di' node voltages are amplified again and relayed to the output-latch. The additional Feed back transistors NMOS\_5 and NMOS\_6 which used for reducing the static loss effect which was suffered by the before comparator design.

### Subthreshold

Subthreshold conduction or sub threshold leakage or sub threshold drain current is the current between the source and drain of a MOSFET when the transistor is in sub threshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage. The terminology for various degrees of inversion is described in Tsividis. In digital circuits, sub threshold conduction is generally viewed as a parasitic *leakage* in a state that would ideally have no current. In micro power analog circuits, on the other hand, weak inversion is an efficient operating region, and subthreshold is a useful transistor mode around which circuit functions are designed.

In the past, the sub threshold conduction of transistors has usually been very small in the *off* state, as gate voltage could be significantly below threshold; but as voltages have been scaled down with transistor size, sub threshold conduction has become a bigger factor. Indeed, leakage from all sources has increased: for a technology generation with threshold voltage of 0.2 V, leakage can exceed 50% of total power consumption.<sup>[3]</sup>

The reason for a growing importance of sub threshold conduction is that the supply voltage has continually scaled down, both to reduce the dynamic power consumption of integrated circuits (the power that is consumed when the transistor is switching from an on-state to an off-state, which

depends on the square of the supply voltage), and to keep electric fields inside small devices low, to maintain device reliability. The amount of sub threshold conduction is set by the threshold voltage, which sits between ground and the supply voltage, and so has to be reduced along with the supply voltage. That reduction means less gate voltage swing below threshold to turn the device *off*, and as sub threshold conduction varies exponentially with gate voltage (see MOSFET: Cut-off Mode), it becomes more and more significant as MOSFETs shrink in size.

Sub threshold conduction is only one component of leakage: other leakage components that can be roughly equal in size depending on the device design are gate-oxide leakage and junction leakage.<sup>[5]</sup> Understanding sources of leakage and solutions to tackle the impact of leakage will be a requirement for most circuit and system designers.

To reduce the sub threshold effect here we use the stacking scheme and design of inverter based amplifier was proposed

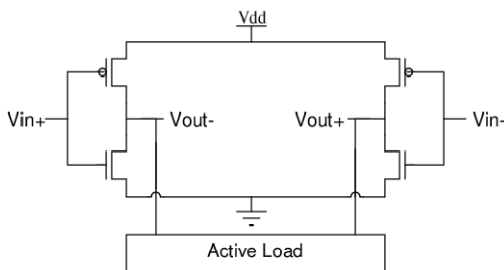


Fig:2 Inverter Based amplifier Design.

The inverter-based amplifier topology shown in Figure 1 uses CMOS inverters as the amplifier input. This input stage design has the advantage of combining the transconductance of the n and p transistors. This combination of the two transconductances should provide 6dB increase in gain over a traditional common source amplification stage, with approximately the same DC bias current. When this architecture is implemented with a standard supply voltage ( $>2v_t$ ), the overall transconductance can be increased significantly depending on how transistors in the inverters are sized and the resulting current through the inverter. High current through the inverter allows significantly high bandwidths to be achieved. Another advantage of this topology is an increase in output swing and linearity when compared to a

traditional common source or cascode amplifier if the respective transconductances of the p and n type transistors are approximately equal in magnitude. For noise, the inverter-based topology offers lower equivalent noise resistance compared to the equivalent common source topology.

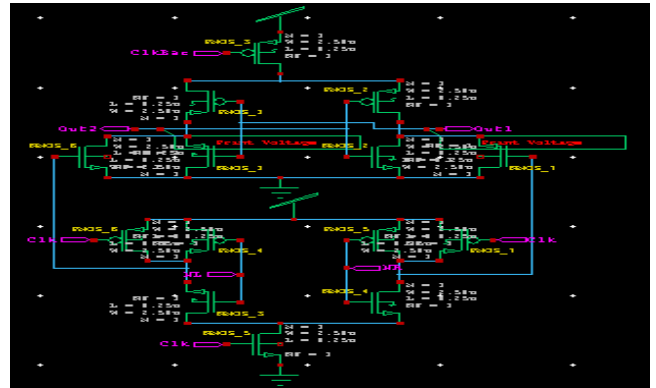


Fig:3. Inverter based amplifier design

Inverter based comparator design operation can be classified as two phases. When  $Clk=0$  the pre-charge transistors are ON state and it changes the fn and fp nodes which makes to turn on the MR1 and Mr2 transistors so that the output was reset to zero at this time the two tail transistors are off state. During the  $Clk=1$  the both fn and fp nodes are charged or discharged their charge due to inputs of INN and INP, this makes the MR1 and MR2 transistors to makes the Latch to switch which in turn makes one output node to 0 and other to 1.

## 4. SIMULATION AND RESULTS

These circuits are designed and simulated using Tanner EDA tool

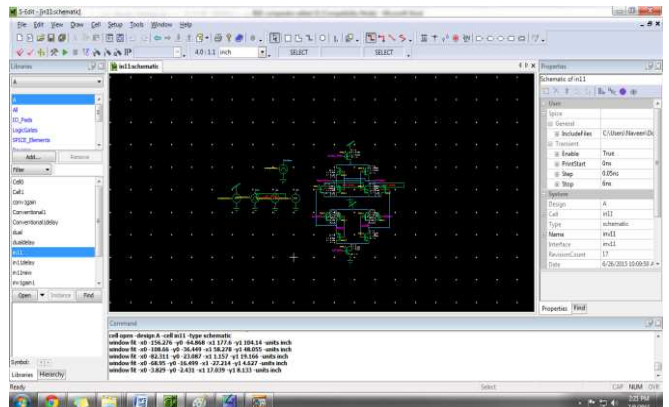


Fig:4: Inverter based amplifier design using S-Edit



Fig.5: Simulation of Inverter based amplifier design

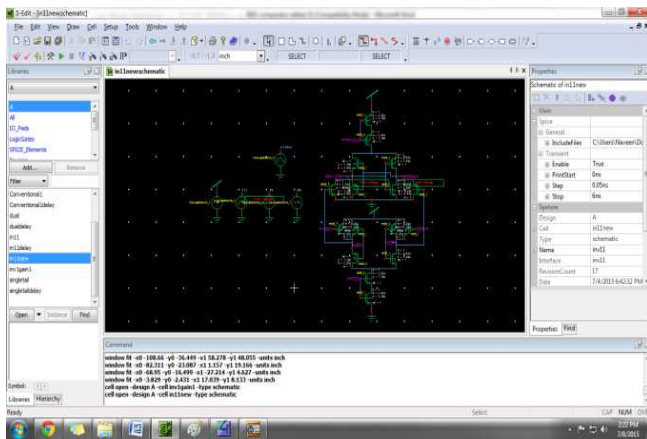


Fig.6: Inverter based amplifier with reduced sub threshold design using S-Edit



Fig.6: Simulation of Inverter based amplifier with reduced sub threshold

## 5. CONCLUSION

In this paper, we presented a comprehensive delay analysis and power analysis for clocked dynamic comparators and

expressions were derived. Two common structures of Inverter based differential amplifier and conventional double-tail dynamic comparators were analyzed. Dynamic latched comparator was designed that works with high speed and low power consumption when compared to double tail latched comparator and pre amplifier based clocked comparator. For comparison we provide analog input to the comparator and the output will be digital. The simulation results show that the proposed circuit inverter based differential amplifier can operate at higher speed with low power dissipation than the other two comparators. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in TSMC018 CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator

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