International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 2, Issue 10, October 2015)

An ALU Optimized for Area and Power

L. KRISHNAVENI[1]
M.Tech in VLSI
Sri Indu College of Engineering & Technology

B. DEEPIKA RATHOD[2]
Associate Professor
Sri Indu College of Engineering & Technology

K. ASHOK BABU[3]
Professor & HOD Dept of EC
Sri Indu College of Engineering & Technology

Abstract: **Power dissipation has a major impact while we are designing any circuit. Since this factor plays a major role in deciding the efficiency of the designed circuit i.e. why in this paper we are proposing a plan for sequential circuits so that we can reduce the power dissipation. Power dissipation which in turn reduces the whole power dissipation of CPU. In this paper, we proposed a low power 1-bit full adder (FA) with 10-transistors and this is used in the design array Multiplier and ALU. The proposed design consists of GDI adder based and mux circuits. By using low power 1-bit full adder in the implementation of ALU, the power and area are greatly reduced to more than 50% compared to conventional design and 30% compared to transmission gates. So, the design is attributed as an area efficient and low power ALU .In this, ALU consists of 4x1 multiplexer, 2x1 multiplexer and full adder designed to implements logic operations, such as AND, OR, etc. and arithmetic operations, as ADD and SUBTRACT. GDI cells are used in the design of multiplexers and full adder which are then associated to realize ALU. The simulation results is done T-Spice tool with TSMC018 technologies.**

Keywords: **GDI, ALU, CPU, Microprocessor, Power, Area, Multiplexer, Full Adder, Multiplier**

1. INTRODUCTION

ALU is one of the main components of microprocessor. They use fast dynamic logic circuits and have carefully optimized structures. Its power consumption accounts for a significant portion of total power consumption of data path [1]. ALU also contribute to one of the highest power-density locations on the processor, as it is clocked at the highest speed and is kept busy most of the time resulting in thermal hotspots and sharp temperature gradients within the execution core. Power dissipation is basically the power which is converted to heat and then conducted or radiated away from the device. Electronic and electric devices can have a limit on the current they can safely handle that is not an electronic limit, but a physical one. For instance, a transistor may otherwise be able to handle a certain amount of current, but it is given a lower current rating because the die gets too hot. Dissipation is usually measured in watts, and uses the usual Ohm's law calculations for power. Most of the Very Large Scale IC (VLSI) applications, Full adder circuit is functional building block and most critical component of complex arithmetic circuits like microprocessors, digital signal processors or any ALUs. Almost every complex computational circuit requires full adder circuitry. The entire computational block power consumption can be reduced by implementing low power techniques on full adder circuitry. In this paper, from different existed base papers several full adder circuits based on different low power techniques have been proposed targeting. We have designed ALU in different way by using GDI cells to implement multiplexers and full adder circuit. The input and output sections consist of 4x1 and 2x1 multiplexers and ALU is implemented by using full adder.

2. NEW GDI TECHNIQUE

Gate Diffusion Input (GDI) method is based on the use of a simple cell. One may be reminded of the standard CMOS inverter at the first glance of this circuit, but there are some important differences: (1) The GDI cell contains three inputs—G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). (2) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased in contrast to CMOS inverter. The basic GDI cell is shown in Figure

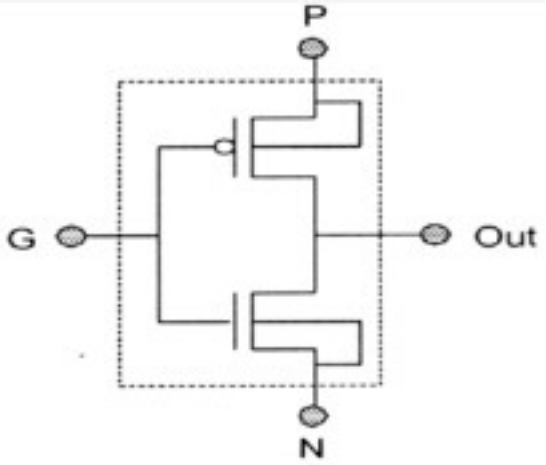


Fig1: Basic Gate Diffusion Input

The circuits required to design Arithmetic and Logic unit are

- **Multiplexer**
- **XOR Gate**
- **Full Adder**

Multiplexer

Multiplexer will acts as a digital switch. Selection line plays a major role to select particular input. If the number of input

International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 2, Issue 10, October 2015)

lines is „2n" and selection lines will be „n" selection lines. With the „n" selection line the particular „2n" input line will be selected. Figure shows the implementation of 2x1 multiplexer and Figure 5 shows the layout of 2x1 multiplexer. The number of selection lines for 2x1 multiplexer is one selection line. With respect to the select line the inputs will be selected. In the same way 4x1 multiplexer also designed to execute arithmetic and logic unit. The number of selection lines required for 4x1 multiplexer is two and with respect to the two selection lines the four inputs will be activated. Figure 6shows the schematic of 4x1 multiplexer and figure 7 shows the layout of 4x1 multiplexer

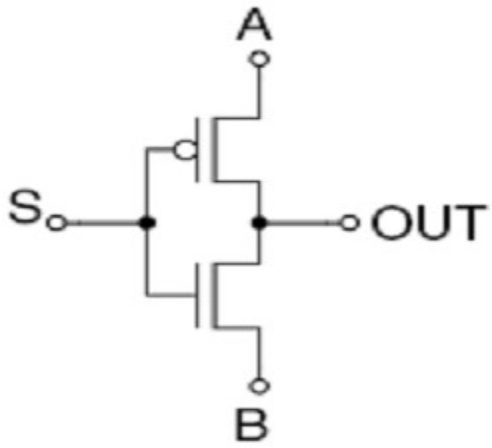


Fig2: GDI based 2x1 Multiplexer

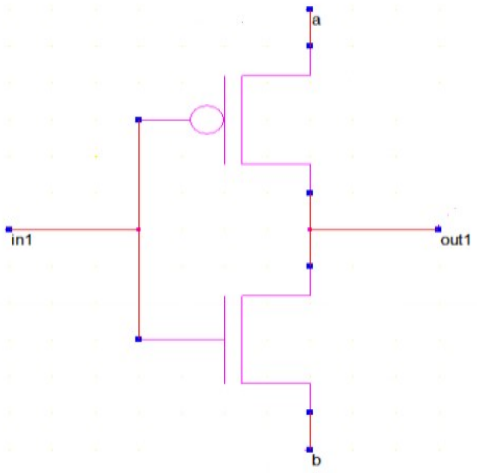


Fig3: GDI based 4x1 multiplexer

XOR Gate

XOR gate is the main building block of the full adder and also which gives the sum output of the full adder. The number of transistors taken to design the XOR gate is four. So the adder circuit can be improved by reducing the area of XOR gate. Figure 8 shows the implementation of XOR gate and Figure shows the layout design of the XOR gate.

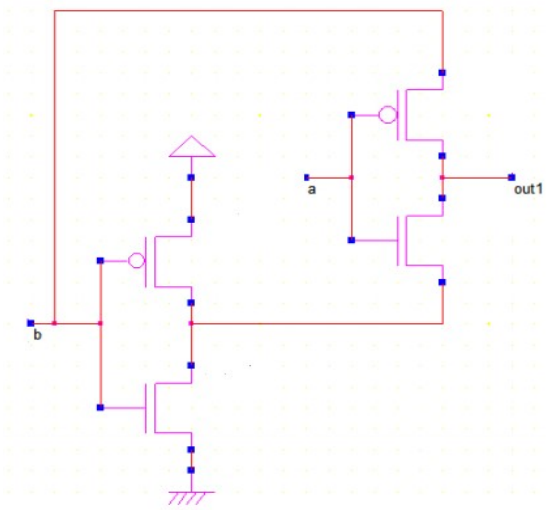


Fig4: GDI based XOR gate

Full adder

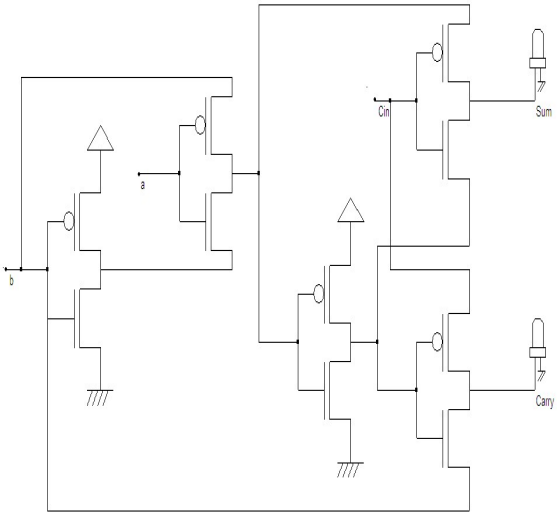


Fig5: GDI based One bit full adder

One bit full adder circuit is also an important block to design Arithmetic and logic unit. Full adder circuit contains three inputs and two outputs named sum and carry. The operation adds only for one bit numbers. The number of transistors required to design one bit full adder are less so the area will be optimized for the better performance of arithmetic and logic unit circuit design. Fig shows the implementation of the one bit full adder and Figure 11 shows the layout design of one bit full adder.

Array Multiplier:

Array multiplier uses and gates Half Adder cell and a Full adder cells

International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 2, Issue 10, October 2015)

3. ALU DESIGN

The Arithmetic and Logic Unit (ALU) is the critical component in the microprocessor it performs all arithmetic like addition, multiplication, subtraction, etc and logical calculations like OR, XOR, AND, NAND. In computer Central Processing Unit (CPU) is the brain of the computer and ALU is fundamental block of CPU. The processor found inside Graphical Processor Unit is also contains powerful ALU. We design ALU using full adder and the multiplexer circuits. The full adder circuits used here is single bit full adder .the multiplexer circuit is of 4X1 mux and 2X1MUX. The full adder circuits are designed PTLGDI logic style. The multiplexer used in the ALU is for input signal selection and to determine what kind operation to performed .The multiplexer is implemented using six and two transistors .the transistor count is reduced and power consumption is also low compared to pass transistor multiplexer. This design is simple in terms of time and area consuming.

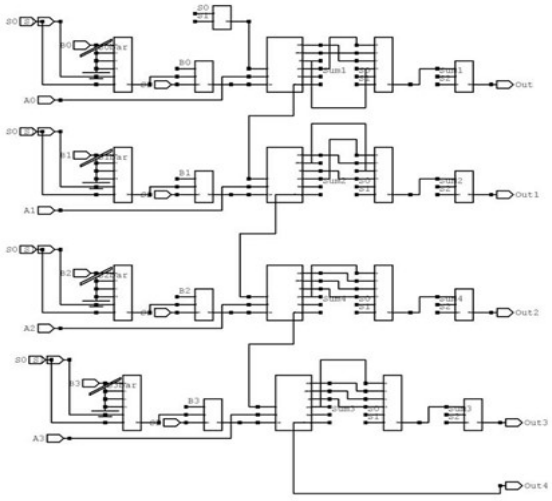


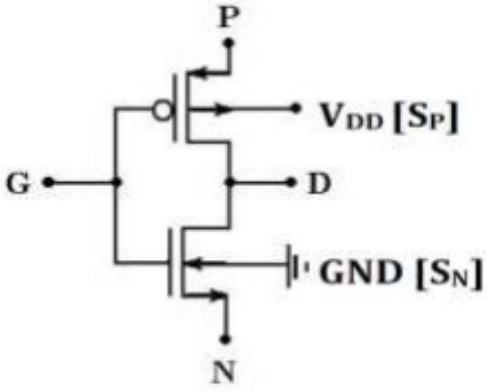
Fig6: ALU design

The full adder performs the computing functions of ALU. The pass transistor logic reduces the parasitic capacitance and GDI logic increase the speed of the operation.

In existing method ALU is designed using 4X1 mux, 2X1 mux and full adder. The multiplexers were designed using pass transistor logic. And the full adder is implemented using 8 transistors. The transistor count is reduced and thus the power

Modified GDI:

Power dissipation becomes most important restriction in high performance applications. Optimizations for basic logic gates are fundamental in order to get better the performance of a variety of low power and high performance devices. These limitations can be overcome by modified gate diffusion input (Mod-GDI) logic styleThis technique allows reducing power consumption, delay and area of digital circuits. Fig 7 shows basic Mod-GDI logic style. In contrast with the basic GDI cell, Modified-GDI [Mod-GDI] cell contains a low-voltage terminal SP configured to be connected to a high constant voltage (i.e. supply voltage) and a high-voltage terminal SN configured to be connected to a low constant voltage (i.e. Ground). Including terminals these ensures that the Mod-GDI cell can be implemented with all current CMOS technologies



Fid 7: Modified GDI Cell

With Modified GDI cell we have designed the Array Multiplier and ALU Unit Their results are compared and shown below

4. SIMULATION AND RESULTS

Theses circuits are designed and simulated using Tanner EDA Tools

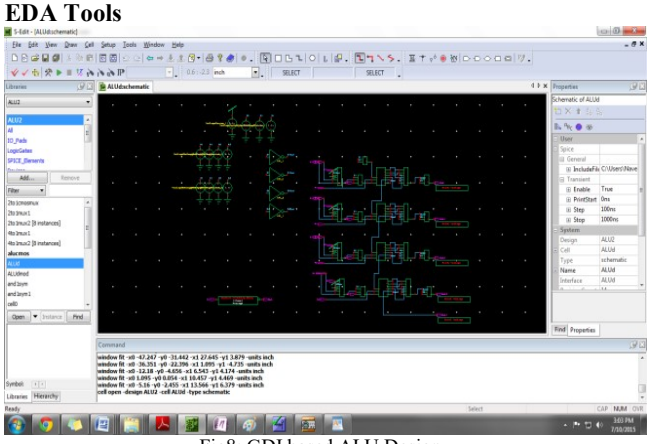


Fig8: GDI based ALU Design

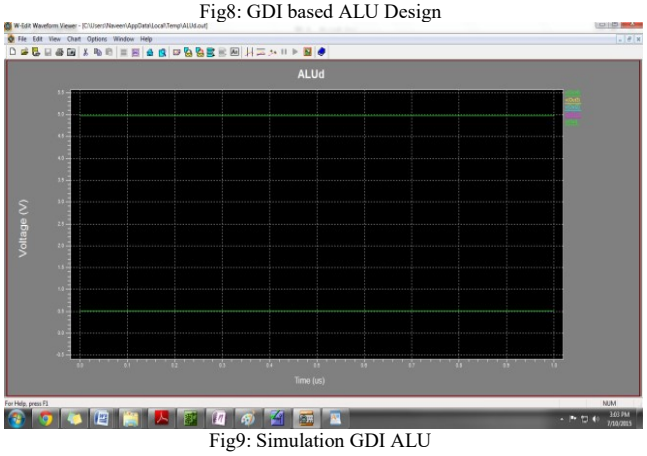


Fig9: Simulation GDI ALU

International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 2, Issue 10, October 2015)

CONCLUSION

In this project an approach is presented for minimizing power and delay for digital circuits. Complex functions can be implemented using this technique using less number of transistors. The leakage power and switching power of Mod-GDI gates is lower than the traditional logic styles. It was shown that the modified GDI though consumes less power than standard GDI technique; it is still can be considered as low power when compared to CMOS logic.

All Simulations are performed through Tanner EDA 13.0 tools. Mod-GDI XOR based array multiplier has least power and delay compared to Mod-GDI XNOR array multiplier. In ALU application GDI has more power and delay. The disadvantage in this project is swing output.

REFERENCES

[1]. J. Han and M. Orshansky, "Approximate computing: an emerging paradigm for energy-efficient design," in ETS'13, May 2013.
[2]. R. Hegde and N.R. Shan hag, "Soft digital signal processing," IEEE Trans. VLSI Syst., vol. 9, no. 6, pp. 813–823, 2001.
[3]. Vaibhav Gupta, Debabrata Mohapatra, Anand Raghunathan," Low-Power Digital Signal Processing Using Approximate Adders" IEEE Trans. on CAD Of IC and Systems, vol. 32, no. 1, Jan 20
[4]. P. Kulkarni, P. Gupta, and M. Ercegovac, "Trading accuracy for power with an underdesigned multiplier architecture," in Proc. 24th IEEE Int. Conf. VLSI Design, Jan. 2011, pp. 346–351.
[5]. V. Gupta, D. Mohapatra, S. P. Park, A. Raghunathan, and K. Roy, "IMPACT: Imprecise adders for low-power approximate computing," in Proc. IEEE/ACM Int. Symp. Low-Power Electron. Design, Aug. 2011, pp. 409–414.
[6]. D. Shin and S. K. Gupta, "Approximate logic synthesis for error tolerant applications," in Proc. Design, Automat. Test Eur., 2010, pp. 957–960.
[7]. H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, "Bio-inspired imprecise computational blocks for efficient VLSI implementation of soft-computing applications," IEEE Trans. Circuits Syst. Part I, vol. 57, no. 4, pp. 850–862, Apr. 2010.
[8]. Y. V. Ivanov and C. J. Bleakley, "Real-time h.264 video encoding in software with fast mode decision and dynamic complexity control," ACM Trans. Multimedia Comput. ommun. Applicat., vol. 6, pp. 5:1–5:21, Feb. 2010.
[9]. M. Shafique, L. Bauer, and J. Henkel, "enBudget: A run-time adaptive predictive energy-budgeting scheme for energy-aware motion estimation in H.264/MPEG-4 AVC video encoder," in Proc. Design, Automat. Test Eur., Mar. 2010, pp. 1725–1730.
[10]. E. Lyons, V. Ganti, R. Goldman, V. Melikyan, and H. Mahmoodi, "Full-custom design project for digital VLSI and IC design courses using synopsys generic 90nm CMOS library," in Proc. IEEE Int. Conf. Microelectron. Syst. Edu., Jul. 2009, pp. 45–48.
[11]. J. Choi, N. Banerjee, and K. Roy, "Variation-aware low-power synthesis methodology for fixed-point FIR filters," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 28, no. 1, pp. 87– 97, Jan. 2009.
[12]. G. Karakonstantis, D. Mohapatra, and K. Roy, "System level DSP synthesis using voltage overscaling, unequal error protection and adaptive quality tuning," in Proc. IEEE Workshop Signal Processing Systems,Oct. 2009, pp. 133–138.
[13]. W. Dally, J. Balfour, D. Black-Shaffer, J. Chen, R. Harting, V. Parikh,J. Park, and D. Sheffield, "Efficient embedded computing," Computer,vol. 41, no. 7, pp. 27–32, Jul. 2008.

About the authors:

L. KRISHNAVENI[1] Perusing M.Tech in VLSI from Sri Indu College of Engineering & Technology.

B. DEEPIKA RATHOD[2] Working as an Associate Professor in ECE in Sri Indu College of Engineering & Technology

K. ASHOK BABU[3], Currently working as professor & HOD Dept of ECE in Sri Indu College of Engineering & Technology.