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VHDL IMPLEMENTATION OF DDS SYSTEM USING BPSK MODULATION

RAHEMUNNISA
M.Tech student, Digital Communication & Networking
Godutai engineering college for women
Gulbarga, Karnataka, India
rahemunnisa786@gmail.com

VANITA KABA
Assistant Professor, Dept. of E&CE, DCN,
Godutai Engineering College For Women,
Gulbarga, Karnataka, India
vbkaba@gmail.com

***Abstract*- Digital Down Sampling is the inverse process of interpolation. This is a technique by means of which the sampling rate of the signal is reduced. This is also known as the decimation process. Down sampling is a form of digital signal compression that finds wide range of applications, but most significantly it finds application in digital communication where reduction of sampling rate results in better bandwidth utilization. Several past works have focused on developing better techniques for digital down sampling. In this work we propose a real time digital down sampling with Xilinx and show an application in BPSK modulation scheme. We show that the bit rate can be decimated to a factor of ten and yet the received signal can be efficiently decoded. In the proposed work we show the digital modulation process using BPSK modulation. Firstly one series of sinusoidal signal samples are stored in the memory. The system accepts three bit binary input signal. This is modulated by first converting the signal to NRZ signal followed by multiplying the signal with repetitive cycle of the sinusoidal carrier. The resultant modulated signal is then down sampled by first applying first order low pass filtering and then down sampling the signal by interleaving. In many of the past works the up sampling is performed by suitable interpolation technique. In this work we show that using signal repeater can easily generate the modulated signal which can then be demodulated by a matched filter. Our contribution to the work is linear interpolation for matched filter in the context of digital down sampling and developing an entire framework for the DDS**

I. INTRODUCTION

Digital down sampler is a system used to reduce the data rate before sending to any person. Communication is the nothing but exchange of information between two or more persons. A basic communication system involves transmitting of information between sender to receiver. This is a multiplier less system and is used to lower the high frequency data. Digital down converter is implemented using FPGA. A Field Programmable Gate Array (FPGA) is an integrated circuit for digital logic or computer. As the name suggests, it is a gate array which is nothing but programmed within the field. Programmable gate array is an array of logic blocks and routing channels. The most common way to implement digital down sampler on FPGA is to use Hardware Description Language (HDL). At the transmitter end information or signal is first modulated and up sampled. At the receiver end the received signal or information is first down sampled by specified decimation factor and then demodulated. Receivers can be in analog form or in digital form. But most oftenally digital system is being used, because of its flexibility and efficient performance. Digital Down-Sampler (DDS) is a important part of radio receivers. The DDS involves the frequency conversion which is necessary to convert the high input sample rates in a radio receivers, down to lower sample rates for simple implementation. The major contribution of this work is to provide the exact framework for digital down sampling in the context of BPSK modulation scheme. The work shows that in digital phase based modulation scheme, time domain re sampling can be adopted as an efficient technique for down sampling. The method can down sample the signal without complex domain filter. Our contribution is also to implement the low pass filtering scheme with delay based circuit. The system utilizes minimum memory and demonstrate that repeater circuit can be used as an effective up sampling scheme for digital up sampling to up sample the signal scale at the receiver side. Proposed system contributes towards the overall architecture for digital down sampling in digital communication system with proof of concept through both timing simulation as well as the signal level simulation.

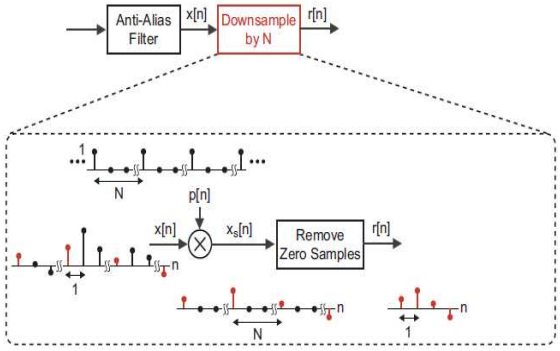

Fig1. General Block Diagram for the Proposed Technique

II. PREVIOUS WORK

Previously deals with FIR filters, these are employed with digital down sampler to down convert the signal by means of reducing the redundant data present in the information signal. Modulating of the incoming information signal will lead to increase the maximum errors. Here the goal is to reduce the maximum error present in the signal. This is the difference

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between original signal and the modulated signal. The two main stages of digital down sampler is the modulating, filtering and second is the down sampling. This paper includes multistage filters and a down sampler. The modulated signal is filtered by adding modulated signal with delayed version of that. And then it is down sampled by a factor M. M is the factor by which the signal will going to reduce the sampling rate. This paper conforms that digital down sampler can be used in mobile communication system. Which will transmit the information from base station to a mobile receiver. By reducing the sampling rate the system will longer distance with more accurate results and with less interruption between users. Now days it can be worked with next generation technologies such as 3G, 4G and 5G.Because the mobile communication is being used so widely, the Goal this paper is to use this digital down sampler with advanced technologies and also with reduced cost so that any one can access it, because the complexity in design and implementation is reduced

III. PROPOSED WORK

First the input signal is converted into NRZ signal. In this particular case the NRZ signal is input from user. The signal is extended by converting to a pulse signal which is discussed in previous chapter. With every signal clock, the signal is multiplied with a carrier , which results in the modulated signal. The signal is down sampled using inter leaver and up sampled using repeater at the receiver. The overall block diagram is shown in figure 2. Non-return to zero is a encoding technique which is used in slow speed communications for both synchronous and asynchronous transmission. In NRZ logic 1is sent as high, and logic 0 is sent as low value. A system output represented with the source signal is called impulse signal. The disadvantage of this is that it contains low energy it can't be sent to longer distance. The impulse signal is converted to square pulse, because it consists of high energy. So that the signal is transmitted over a longer distance. Modulation is the process of adding the information of the signal. Here the pulse signal is get multiplied with carrier signal. Modulation is done in sequence by sequence order. A low pass filter is a filter which passes information with a lower frequency than it will ignore frequency higher than cutoff frequency. Here filtering is done by adding BPSK signal with the delayed version of that signal. Down sampling is the process of reducing the sample rate, when transmitting over a longer distance. Down sampling mainly depend on the factor down sample depth, by which factor down sampling is to done. Here down sampling by ratio of 10. Up sampling is done at the receiver. This is the process of adding the zero valued samples to a down sampled signal to increase the sampling rate. Demodulation is the process of extracting the original information from the carrier signal.DDS demodulation is done by multiplying the up sampled signal with carrier wave. Decoding is the inverse process of encoding, decoder converts encoded signal back to original information. The last step is the matched filter, the signal from the decoder is given to matched filter which will increases the signal to noise ratio.

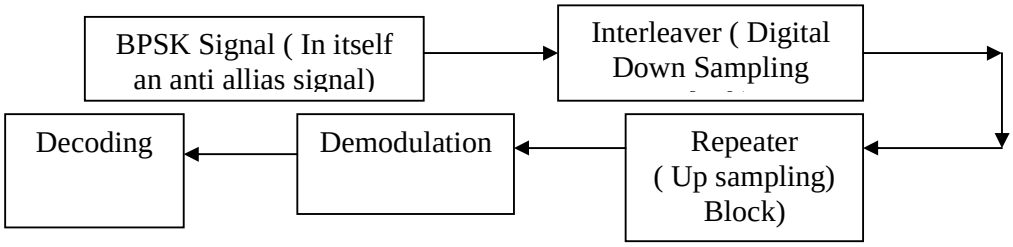

Fig 2. Block diagram of proposed system

Sampling Theory

An analog signal is sampled over time. The sampling process selects a values at equal interval of time. As the time difference between two consecutive samples decreased, the signal is better approximated towards the analog signal. Once the signal is sampled, it needs the ability to be stored. Even the sampled signals may have infinite levels. Hence the signal must be quantized with a fixed number of bits. Sampled signals are approximated by the near by quantization value. That is not shown in this image.

Figure 3 also shows the down sampling. Down sampling is done by further re sampling the signal and selecting only 1/k of n samples. Down sampled signal is processed by a DSP unit before upsampling. At the receiver, the signal is first processed with a suitable filter and then is upsampled to obtain the original signal. This is also known as interpolation. Interpolation process attempts to find the missing samples and then append them between the down sampled signal to finally obtain the near analog signal back

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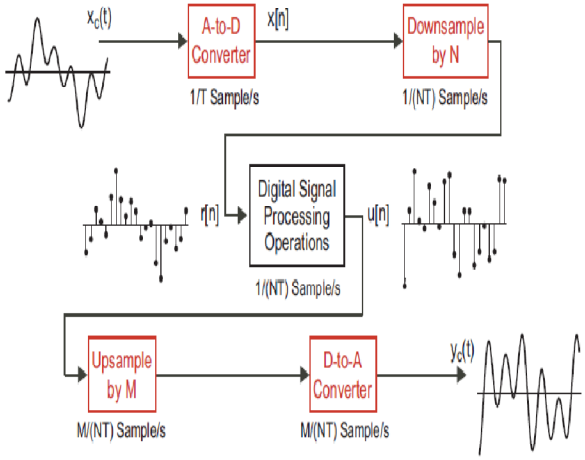

Fig 3. Block diagram of down sampling

Filtering Operation

Figure 4 introduces the filtering block over the figure 3. The filtering is Anti aliasing filter. Under sampling results in aliasing effect. Anti aliasing filters essentially corrects the phase of the signal such that over lapping of the block of the signal does not appear on the signal.

The process of recovery includes interpolation which deals with finding the missing samples which were lost due to the process of under sampling. In this work we perform repeaters as the interpolation process. There can be however more complicated interpolators starting from complex time series interpolator to predictive filters.

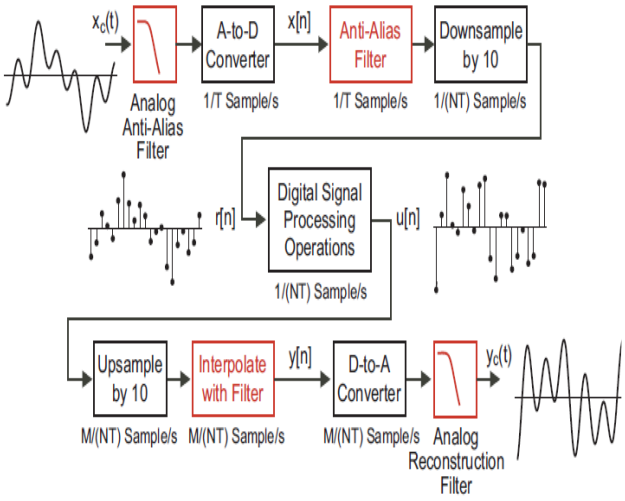

Fig 4. Block diagram of Filtering

IV. MATLAB RESULTS

The proposed designs are simulated in Xilinx 12.1 and the outputs are shown below. Experimental results shows the complexity has been reduced with decrease in chip area .

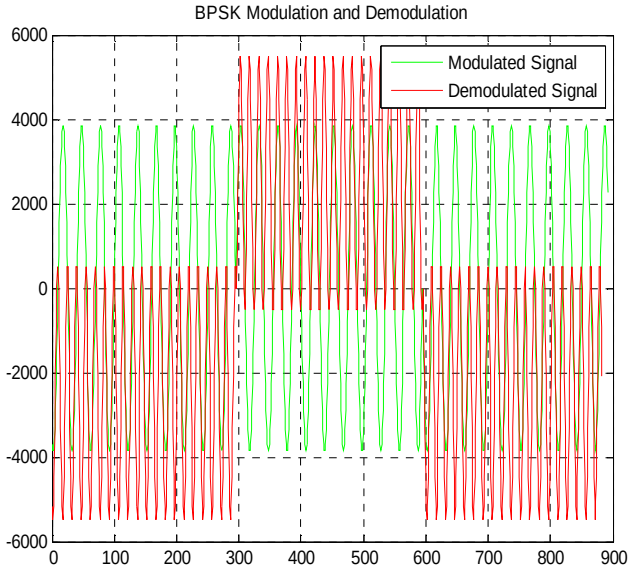

Fig5 BPSK modulation&demodulation

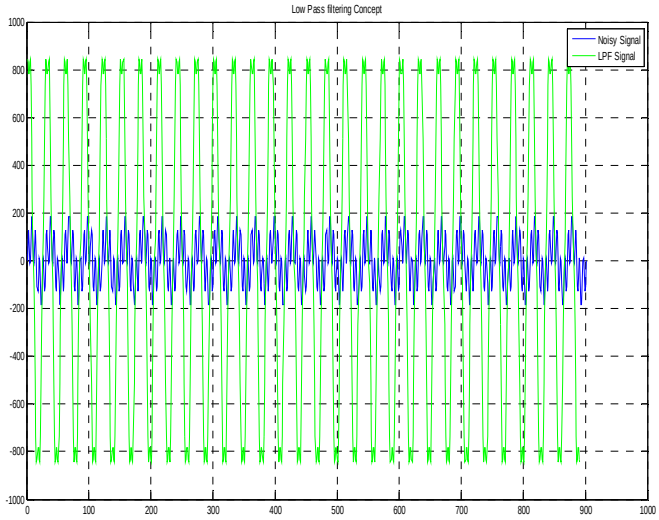

Figure 6 shows low pass filtering concept

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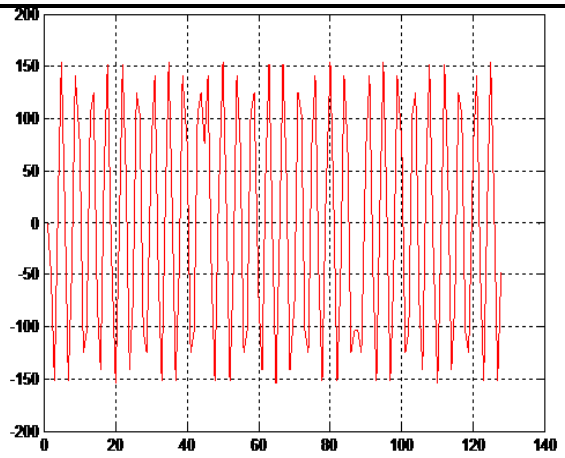

Figure 7 shows down sampling

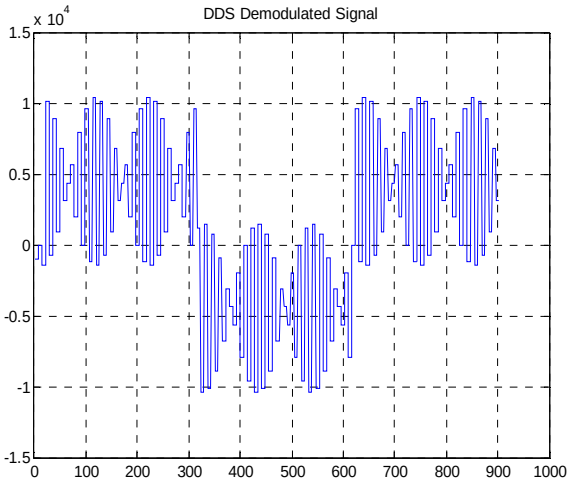

Figure 8 shows DDS demodulated signal

VHDLSIMULATION RESULTS

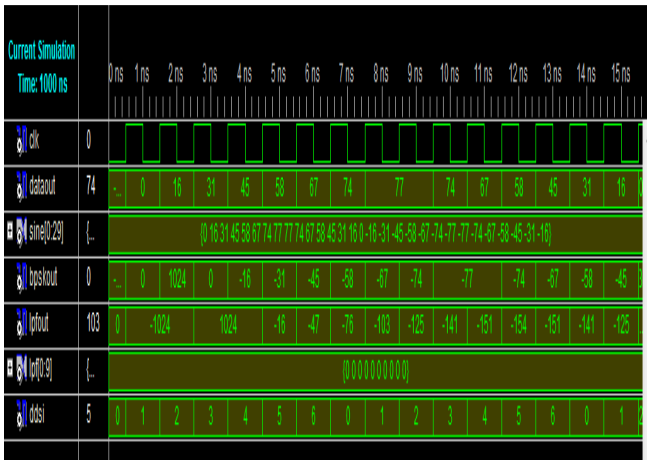

Figure 9 shows VHDL waveforms for DDS

V- CONCLUSION

In this work we have developed a unique digital down sampling solution for BPSK modulation system. We have been able to eliminate the complexities of anti aliasing filter and repeaters by utilizing the basic properties of the modulated signal. We have argued and justified the proposed design. We have further simulated the system using VHDL and justified the timing diagram. The result is also written back in file and the data is represented by MATLAB program as VHDL simulator can not display the analog interpretation of the signal. Our work has proved that proposed system can be effectively used in digital modulation schemes, especially phase based modulation schemes, in order to maximize the channel utilization.

REFERENCES

[1]. K.S.Sushmitha, G.Vimala Kumari, International Journal of Engineering Trends and Technology- Volume3Issue4- 2012, "Implementation of Frequency Down Converter using Multiplier free filter on FPGA".

[2]. Sursumel Singh, International Journal of Engineering Research and Development e-ISSN: 2278-067X, p-ISSN: 2278-800X,Volume 8, Issue 11 (October 2013), PP. 47-50 "Design & Implementation of Digital down Converter for Wcdma System".

[3]. Pratibha Paliwal, Manpreet Singh, International Journal of Advanced Research in Computer and Communication Engineering, Vol.2, Issue 9, September 2013, "Design and Implementation of Digital Down-Converter for Wimax System".

[4]. Puneeth Kumar T.R1, G.Ranjani2, Sirisha Nemani, Paramita Barua, D.Anuradha, R.Kuloor, 9th International Radar Symposium India - 2013 (IRSI-13), "FPGA Implementation of ImpulseSynthesis for Radar Receiver using Digital Down Converter".

[5]. Tom Powers, Roger Flood, Curt Hovater and John Musson, JLAB-ACT-00-07, "Two Applications of Direct Digital Down Converters in Beam Diagnostics".

[6]. Majid Salal Naghmash and Mohd Fadzil Ain, Journal of Engineering and Technology Research Vol.1 (5), pp.091-101, August 2009 Academic Journals "Design of minimum error digital down-converter (DDC) for GSM mask requirements".

[7]. Shu-Ming Tseng, Jian-Cheng Yu, Zheng-Hau Lin, CTRQ 2012 : The Fifth International Conference on Communication Theory, Reliability, and Quality of Service, "Software Digital-Down-Converter Design and Optimization for DVB-T Systems".