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Implementation of SKLANSKY Tree Adder using Quasi Static Adiabatic Logic

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***Abstract*- This paper presents the design for low power circuilts which use reversible logic to conserve energy. The project presents the implementation of a Sklansky tree adder structure using a quasi static adiabatic logic namely CEPAL (Complementary Energy Path Adiabatic Logic). The SKLANSKY Tree adder structure has been chosen due to its increased fan-out that results in reduced latency and improved speed performance. The performance characteristics of the CEPAL tree adder are compared against the conventional static CMOS of 130 nm technology logic is to identify its adiabatic power advantage. In this we design the 4-bit CEPAL and CMOS using Sklansky tree adder and thus results in the 30% of power saving over static CMOS.**

***Keywords*– CMOS, CEPAL, Adiabatic Tree Logic, Static Adiabatic logic, SKLANSKY Tree adder, ERL.**

I. INTRODUCTION

The reversible energy recovery circuits have the control signal(s) coming from the next stage, the design overhead for applying such logic in a large system is considerable. Most of the irreversible adiabatic circuits are, however, referred to dynamic circuit properties which are of higher switching activity and ratioed logic in spite of their advantages. In addition the requirements of multiphase and multi clock operations also make them unfavorable in terms of design complexity and implementation area except for few works. A quasi-static energy recovery logic (QSERL) has been proposed in order to overcome the drawbacks of the irreversible ERL families QSERL features simplicity and static logic-resembled characteristics, which substantially decreases the complexity and switching activity .The employment of only complementary sinusoidal power clocks makes it be provided with higher energy efficiency compared to those of the prior arts utilizing trapezoid or triangular clocking scheme. Despite the advantages, QSERL suffers from in robustness caused by output floating associated with the alternate hold phases in operation .Although the floating can be eliminated by adding clocked feedback keeper to each logic (keeper is turned ON only when QSERL is in the hold phase),there will still be unwanted power loss. Also, the added area overhead as well as control signals would restrict its application. Motivated by this, we propose a complementary energy path adiabatic logic (CEPAL). CEPAL inherits all the advantages of QSERL, but it eliminates further the hold phase for the same operation conditions, thereby not only improving the robustness but also drastically increasing the throughput as a whole. We analyzed the performance of CEPAL through extensive experiments. Different from those studies in the literature, the efficiency of using CEPAL in clocked storage element (DFF) will be explored .In order to provide insights in to difference between the proposed design and other logic styles used for achieving iso-performance, comparing CEPAL vis-a-vis one of the sub threshold logic styles is also elaborated.

II. COMPLEMENTARY ENERGY PATH ADIABATIC LOGIC

The structure of the static energy recovery logic CEPAL employed in our design is shown in Fig 1. It eliminates some of the major problems incurred by the multiphase and multiple clock-operated adiabatic circuits. CEPAL uses two complementary sinusoidal power clocks. The CEPAL consists of two charging and discharging transistors along with Pull-up and Pull down N networks as depicted in Fig. 1. To briefly discuss the operation of the circuit, assuming that the initial output V_{OUT} is high, and a P network is on, while the N network is off, the current output does not switch. In other words, the output node will neither be following the power clock (PC) nor its complement (PCbar), when the next input does not warrant a change in the output node. Let us consider the alternate case, in which a initial output V_{OUT} is low and the P network is on, while the N network is off. Then, the output node V_{OUT} follows either PC or its compliment PCbar, which ever swings to high-level and the output reaches high, it ramps down to low level by following the power clock during its downward transition, hence making the node V_{OUT} to become a floating node. However, this condition is overcome when the compliment of the power clock swings to high level. This eliminates the weak high node condition of the output. This also eliminates the hold state of the other two phase power clock operated circuits [7].

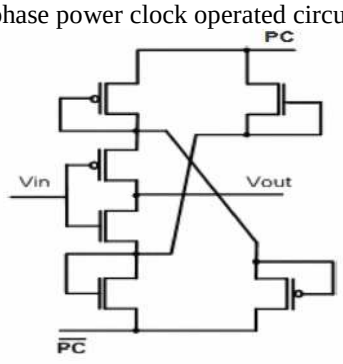

Figure 1: CEPAL Inverter

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The elimination of redundant switching of the output nodes and the consequent reduction in adiabatic power dissipation are the major advantages of these CEPAL [7]. This beneficial characteristic of CEPAL identifies the circuit as the static type. Figure 2 shows the simulation transients of static and dynamic inverter.

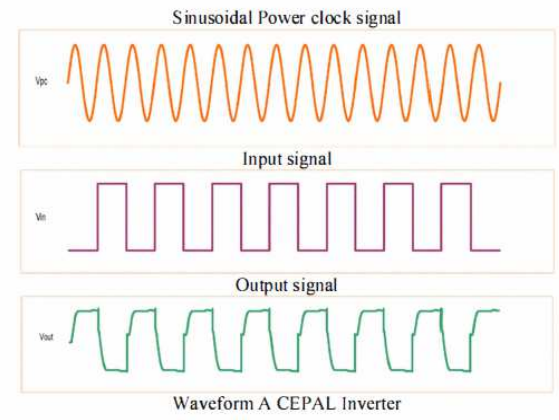

Figure 2: waveform a CEPAL Inverter

III. SKLANSKY TREE ADDER

The SKLANSKY Tree adder structure has been chosen due to its increased fan-out that results in reduced latency and improved speed performance. The tree structures proposed by sklansky adder are the fastest among the already proposed structure and it is also noticed that this structure realizes the advantage in terms of reduction and deduced latency of computation. This paper uses the sklansky tree adder to validate the logic due to its high speed of operation. The schematic design of the circuits using CEPAL AND CMOS are made for the tree adder .this circuit design is done inherit, through the instantiation of the individual modules, such as AND, XOR, OR, BUFFER, AND-OR, AND-OR-AND and PG (Propagate-generate) cells. The individual modules are constructed by using pre-layout simulation through the schematic editor tool and the designs are exported to the Spice circuit Simulator. The operations of these circuits are validated through comparison at various power-clock frequencies and peak power –clock voltages

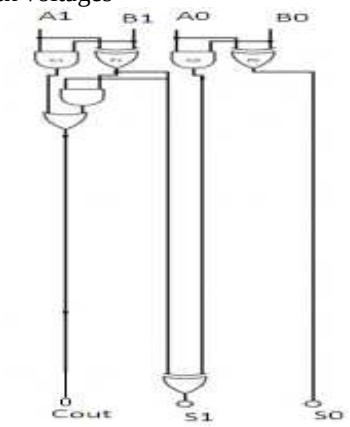

Figure 3: 2-Bit Sklansky Tree Adder

IV. RESULTS AND COMPARISION

The adiabatic tree adder was implemented using 130 nm TSMC process technology files. The simulation results of CEPAL tree adder are compared with the static CMOS. The simulation environment was maintained the same to provide justified results. The simulations were performed for random input patterns applied to the CEPAL tree.

Table.1. Power comparison

Power comparison	CEPAL	CMOS
	28.142µW	3.7441µW

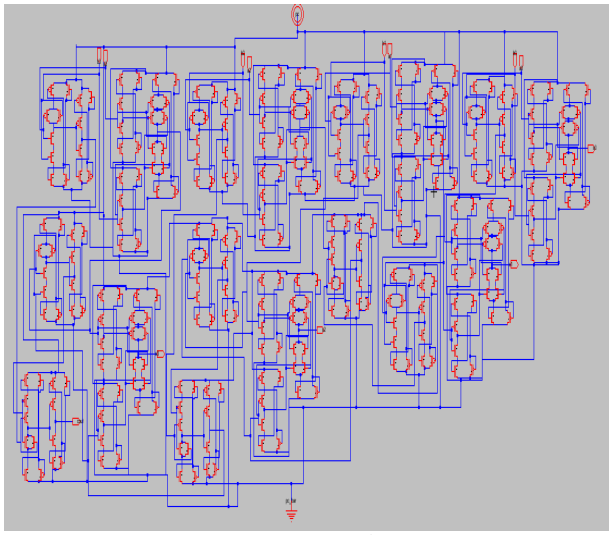

Fig 4: Schematic and simulation results for the 4 bit adder CEPAL

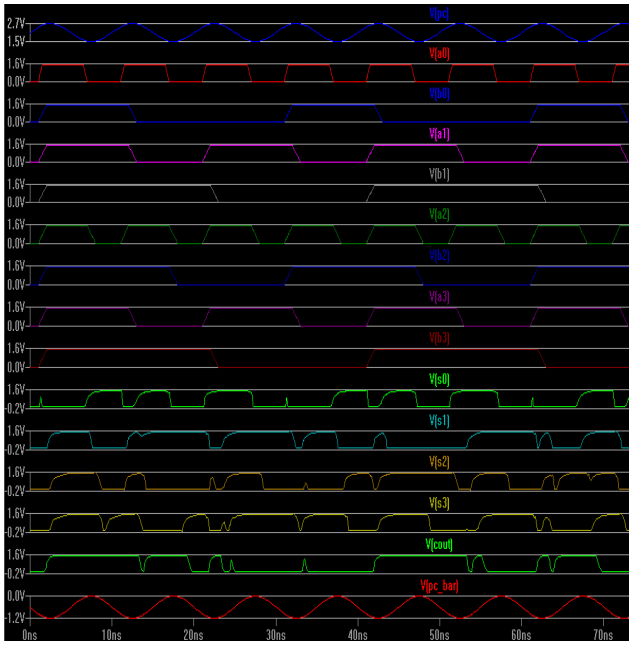

Fig 5: Power Comparison for CMOS and Cepal

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Fig 6: CMOS Power

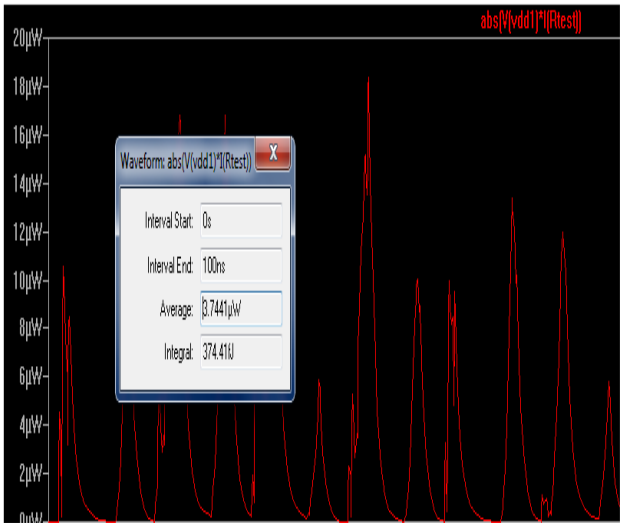

Fig 7: CEPAL Power

VI. CONCLUSION

In this paper, we have presented the implementation of 4 bit Sklansky tree adder circuit using adiabatic logic family, namely, CEPAL. The CEPAL structure, being a static type of logic, inccurs the reduced switching activity than the dynamic adiabatic logic. This is, however, is found to be realized at the cost of increased fan-out node capacitance values. Simulations indicate that the CEPAL realizes energy advantage against the static CMOS to the tune of 30%. The results also prove that the CEPAL is suitable for optimal speed performance applications.

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