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Design and Implementation of a Costas Loop for Wireless Protocols on FPGA

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***Abstract*— In this paper, the design of a Costas loop, based on the principle of digital Costas loop, is described. The numerically controlled oscillator (NCO) is designed using the CORDIC algorithm, instead of the look-up table (LUT) approach, which reduces the memory requirement. The low pass filters and the loop filter are designed with minimal number of multipliers. In order to validate the scheme, simulation is performed using MATLAB and Modelsim simulator. The simulation results show that the loop is stable and performs demodulation correctly. The whole design is implemented on FPGA.**

***Index Terms*— Costas loop, CORDIC, FIR filter, multipliers, FPGA**

I. Introduction

Wireless communication systems provide long range communication services, which are impractical to provide in the case of wired systems. The transmitter and receiver which may be few hundreds or thousands or even millions of kilometers apart, communicate through a wireless channel by means of unguided electromagnetic wave propagation. The message signal transmitted from the transmitter is modulated with a carrier to strengthen the signal, so as to enable long distance propagation. At the receiver, the demodulation process has to be performed on the received signal in order to recover the message signal. For this purpose, the Costas loop method is commonly used, as the prime use of Costas loop is in wireless receivers. The receiver must capture and track the carrier of the input. When the loop is locked, both the carrier extraction and the demodulation processes take place and the demodulated output is obtained [1]. Therefore, the Costas loop method has a wide use in practical applications [2].

An all-digital Costas loop has been realized [3], and in order to validate the scheme, simulation is performed on MATLAB and Modelsim platform. Further, the design has been implemented on FPGA [4, 5].

II. Principle Of Costas Loop

The Costas loop is used to obtain a synchronous receiving system. It is used to maintain synchronization between the carrier wave and the local oscillator. The loop consists of numerically controlled oscillator, multiplier, low pass filter, phase detector and loop filter. A block diagram is shown in Fig. 1.

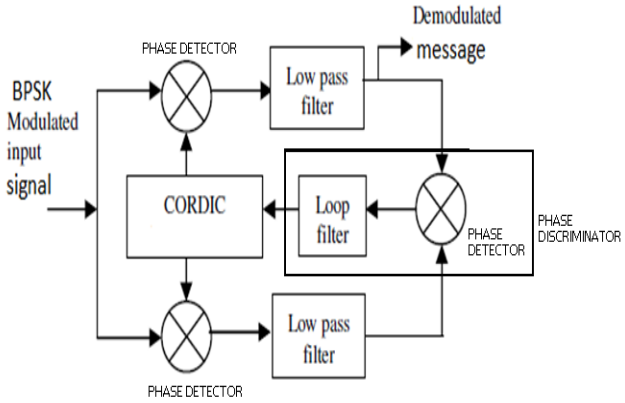

Fig. 1: Block diagram of Costas loop

The modulated input signal is fed to the two phase detectors, I-channel and Q-channel respectively. The local oscillator also supplies an input signal to each of the phase detectors, which are out of phase by 90 degree. The output of the multipliers are passed through low pass filter and given to a phase discriminator, which consists of a phase detector followed by a loop filter. Output signal produced by the phase discriminator is proportional to phase error. This output signal is to correct the phase error in the oscillator, thus obtaining synchronization between the carrier and the NCO [6].

III. Design of Costas Loop

A message signal, which is a square wave of 200Hz and a carrier signal, which is a sinusoidal signal of 2000Hz are used to obtain a modulated BPSK message signal. This BPSK signal is given as the input to the Costas loop. The same message signal is fed to both the product detectors.

A. Design of NCO

The NCO outputs two signals that are out of phase by 90 degree. One is a sinusoidal signal and the other is a cosine signal. The sinusoidal signal is fed to the I- channel phase detector and the cosine signal is fed to the Q-channel phase detector.

The NCO is designed using the COordinate Rotation DIgital Computer algorithm [7]. CORDIC is a hardware efficient algorithm to calculate trigonometric and hyperbolic functions [8, 9, 10]. It does not make use of hardware

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multipliers, thus consuming less power. It makes use of addition, subtraction, bit shift and table look-up instead of multiplication for its operations. This method provides the advantage of decreased memory requirement compared to the LUT approach.

The algorithm is used to obtain a sinusoidal and cosine signal. Vector rotation is considered as a base for all trigonometric functions. Firstly a vector (x, y) is considered, which is rotated in the Cartesian plane with the angle θ. The rotation operation is decomposed into successive basic rotations. Each basic rotation is realized with shift-and-add arithmetic.

In order to find the sine and cosine value of an angle, iterative rotations of the vector (x, y) is performed in the Cartesian plane, about a unit circle. The resulting x- coordinate gives cosθ value and y-coordinate gives sinθ of the given angle. This is shown in Fig. 2.

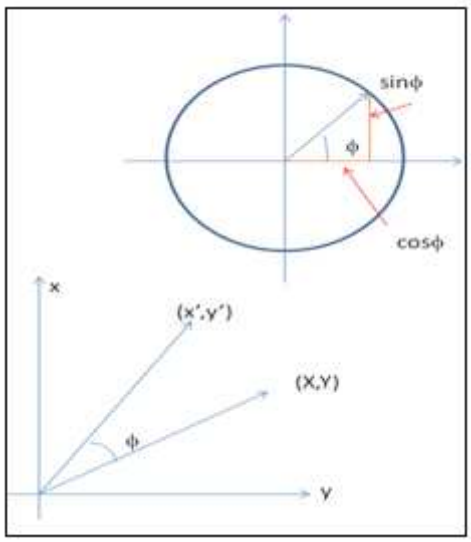

Fig. 2: Basic operation of CORDIC

11 iterations are performed in this project, to obtain a precision of values up to 4 decimal places.

The equations involved in performing the iterative rotations are:

$$x_{i+1} = k_i\ (x_i-(y_i d_i 2^{-i})) \quad (1)$$

$$y_{i+1} = k_i\ (y_i+(x_i d_i 2^{-i})) \quad (2)$$

Where, d_i is the decision Given by,

$$d_i = \begin{cases} -1, \text{ if } z_i < 0 \\ 1, \text{ otherwise} \end{cases}$$

And k_i is the gain.

Z_i keeps track of the angle that has been rotated and is given by:

$$z_{i+1} = z_i - d_i \tan^{-1}(2^{-i}) \quad (3)$$

The sine and cosine values obtained from the CORDIC algorithm have high precision compared to the LUT approach. CORDIC approach minimizes the number of gates needed to implement the required functions, thereby making it suitable for FPGA implementation.

B. Design of Phase Detector

The phase detectors have been designed using Baugh Wooley multiplier to perform signed multiplication, as shown in Fig. 3. The Baugh Wooley multiplier uses very less number of logical operations to perform multiplication and is best suited for signed inputs than other algorithms.

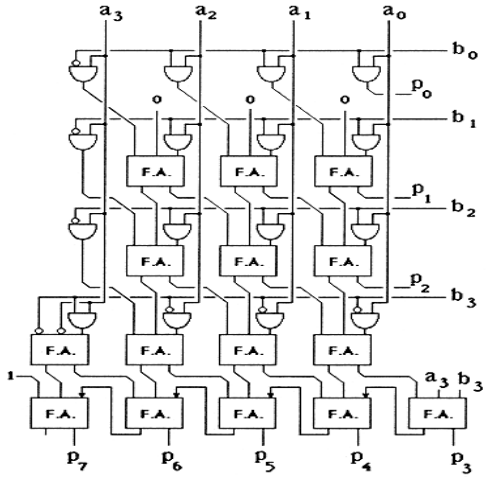

Fig. 3: Architectural block diagram of the Baugh-Wooley multiplication algorithm

C. Design of LPF

The outputs from the phase detectors are fed to the LPFs. The low pass filters are used to filter out the high frequency components and noise present in the signal, and are realized using FIR filters. The FIR filters are stable and provide a finite impulse response. The LPFs have been designed with minimal number of coefficients/multipliers. Symmetric coefficients are considered. Each LPF is designed with just 9 multipliers in the MATLAB simulation, which are further reduced to 5 multipliers in the Verilog coding. This provides the advantages of reduced number of calculations and memory requirement.

D. Design of Phase Discriminator

The phase discriminator consists of a multiplier followed by a low pass filter. The LPF is realized using FIR filter. The phase discriminator is used to obtain the phase error. The DC control signal produced by the phase discriminator, which is proportional to the phase error, is used to correct the phase in the local oscillator. Thus, the phase discriminator maintains the NCO in sync with the carrier wave.

IV. Simulation and Results

The simulation is performed using MATLAB and Modelsim based on the design discussed above. The modulated

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BPSK signal obtained by multiplying the message signal with high frequency carrier is as shown in Fig. 4.

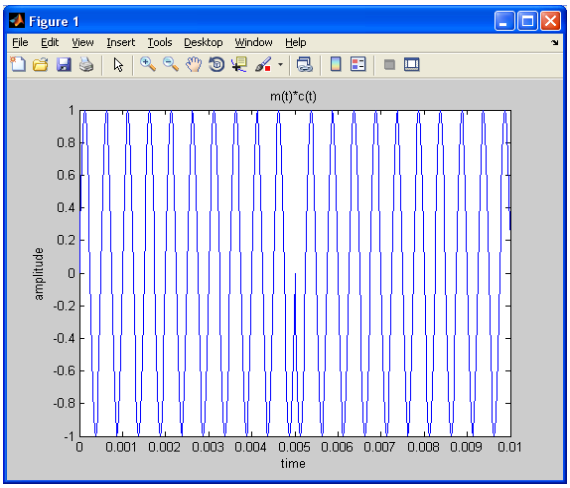

Fig. 4: Modulated BPSK signal

The sine and cosine signals generated using CORDIC algorithm as the output of NCO is shown in Fig. 5.

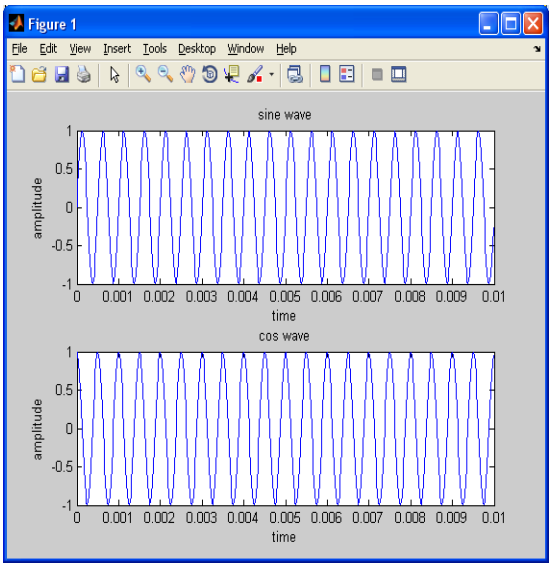

Fig. 5: Sine and cosine waves generated using CORDIC algorithm

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The modulated input signal and the output signals of the NCO are multiplied and the resulting output of the phase detector is as shown for both I-channel and Q-channel, in Fig.6.

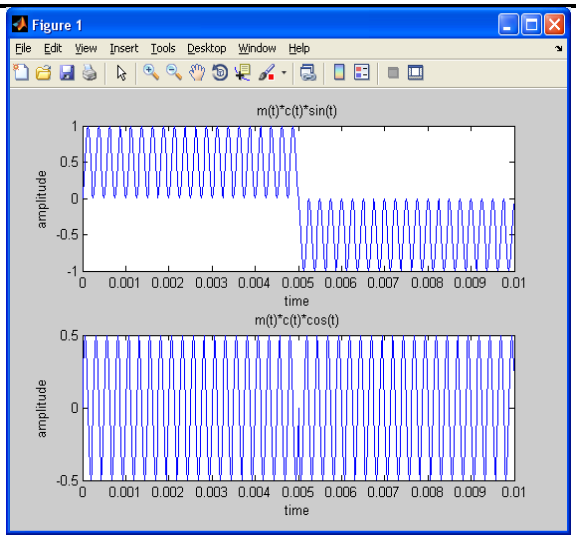

Fig. 6: Output of I-phase and Q-phase product detector

The outputs of phase detector are passed through LPSs to remove high frequency components and noise. The resulting output after filtering is shown in Fig. 7.

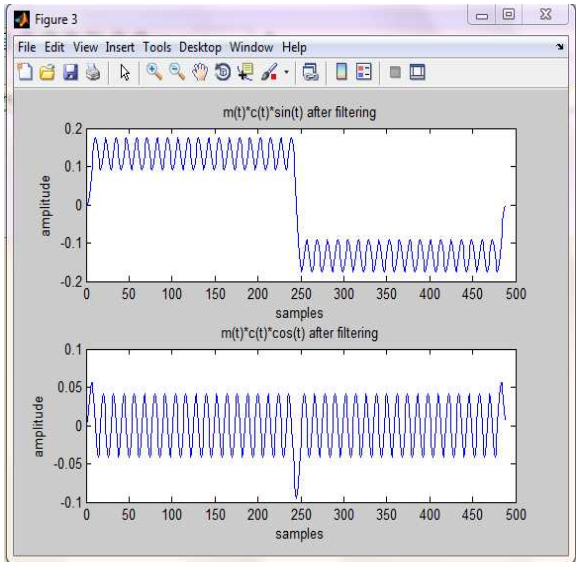

Fig. 7. Outputs of LPFs

After filtering, the resulting signals are fed to the phase discriminator. The output of the phase discriminator gives the phase error. As we can see in Fig. 8, the output indicates a negligibly small value, almost equal to zero. This shows that the phase error of the Costas loop is zero and hence, the loop is locked.

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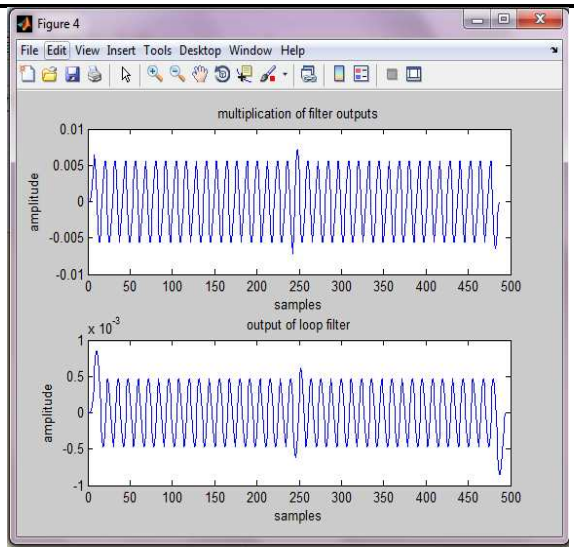

Fig. 8:Output of the phase discriminator

The Modelsim simulation is as shown below in Fig. 9.

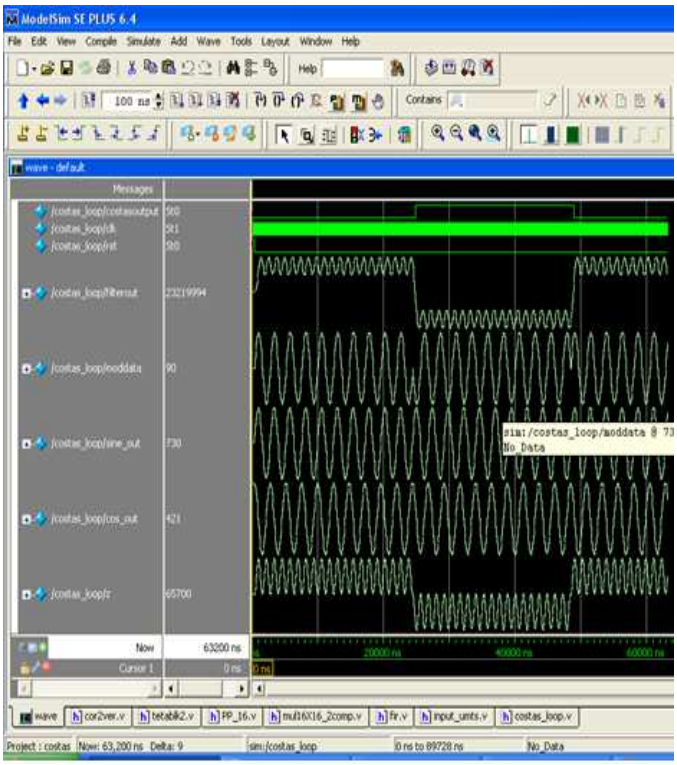

Fig. 9: Modelsim Simulation results

The design is then implemented on a Spartan II Fpga kit, whose output is viewed through the Chipscope analyzer.

V. Conclusion

Through the analysis of principle of digital Costas loop, a method of design and implementation of Costas loop has been proposed. The numerically controlled oscillator (NCO) is designed using the CORDIC algorithm, which provides the advantages of increased precision and of decreased memory requirement, compared to the look-up table (LUT) approach. CORDIC does not make use of multipliers, it performs computations based on bit shift, addition, subtraction and table look up operations. Thus, it is hardware efficient. The filters have been designed using minimum number of multipliers. Lower the number of multipliers in the design, lesser is the number of calculations, memory required and the power consumption. The simulation results show that the loop is stable and performs demodulation correctly. Further, the design has been realized on a Spartan II FPGA and the results have been tested and verified. This method provides the advantages of easy implementation and integration. Further, the loop can be implemented in the demodulator module of wireless systems for various applications.

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References

[1] Shamla B, Gayathri Devi KG, “Design and implementation of Costas loop for BPSK demodulator”, Dept. of Electron. & Commun., Gov. Eng. Coll., Thrissur, India, 2012.
[2] Ziheng Yang, Yuan Bai, Zhongjun Zhao, “Design and implementation of digital Costas loop based on software defined radio”, Electron. Eng. Colleges, Heilong Jiang Univ., Harbin, China, 2011.
[3] Kumm M, Klingbeil H, Zipf P, “An FPGA-Based Linear All-Digital Phase-Locked Loop”, Univ. of Kassel, Kassel, Germany, 2011.
[4] Lia Gong Guo, Ming San, Jun Cai, “Simulation and implementation of Costas loop based on FPGA”, Coll. of Electrical & Information Engineering, An Hui University of Science & Technology, Huainan, China, 2011.
[5] Huimei Yuan, Xiasoguag Hu, Juong Huang, “Design and implementation of Costas loop based on FPGA”, Coll. of Inf. Eng., Capital Normal Univ., Beijing, 2011.
[6] A P Godse, U A Bakshi, “Analog communication”, Technical Publications, Pune, First Edition 2008.
[7] Lei Wang Weilian, “The design of NCO based on CORDIC algorithm and implementation on FPGA”, Sch. of Inf., YunnanUniv., Kunming, China, 2011.
[8] Samuel Ginsberg, “Compact and Efficient Generation of Trigonometric Functions using a CORDIC algorithm”, Cape Town, South Africa, January 2002.
[9] Herdert Dawid, Heinrich Meyr, “CORDIC Algorithms and Architectures”, Aachen University of Technology, Germany, 1992.
[10] Ray Andraka, “Survey of CORDIC Algorithms for FPGA based computers”, Ray Andraka, New York, USA, 1998.