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Design and Implementation of Phase Locked Loop using Current Starved Voltage Controlled Oscillator in GPDK 90nM

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***Abstract*— Phase Locked Loop is the heart of the many modern electronics as well communication system. Hence there is necessity of a PLL which must operate in the GHz frequency range. PLL is a mixed signal circuit as its architecture involves both digital and analog signal processing units. This paper focus on design of High-Speed, Low Power Consumption, faster face and frequency locking PLL. All micsellious blocks of PLL had been designed in GPDK 90nm CMOS Technology with supply voltage 1.8V using CADENCE spectre tool. Virtuoso Analog Design Environment tool of Cadence have used to design and simulate schematic. Simulation results were done for all process corners, temperature (-40˚C to +100˚c). It is found that designed PLL consumes 865.5 uw power and have a lock time 100 ns.**

Index Terms—**: Phase Locked Loop (PLL), Phase Frequency Detector (PFD), Charge Pump (CP), Low Pass Filter (LPF), Current Starved Voltage Controlled Oscillator (CSVCO), Frequency Divider.**

I. INTRODUCTION

The most versatile application of the phase locked loops (PLL) [1] is for clock generation and clock recovery in microprocessor, networking, parallel and serial data communication, and frequency synthesizers. Because of the increase in the speed of the circuit operation, there is a need of a PLL circuit with faster locking ability. Many present communication systems operate in the GHz frequency range. Hence there is a necessity of a mixed signal PLL [1] which must operate in the GHz range with less lock time. The PLL performance depends upon its order. If 'n' is the order of loop filter than 'n+1' is the order PLL [2]. The stability of the whole PLL system depends on the order of the loop filter. The voltage controlled oscillator (VCO) is the heart of the PLL. The present work focuses on the redesign of a PLL system using the 90nm technology. Hence a current starved ring oscillator has been considered for its superior performance in form of its low chip area, low power consumption and wide tunable frequency range. The PFD has been considered for its fast acquisition capability.

II. PHASE LOCKED LOOP (PLL)

This section consists of details circuit architectures of Phase locked loop.

Phase locked loop is mostly used in wireless communication and data recovery circuits. At present for above mentioned application a low voltage low area and high performance integrated circuits are used which complicates the implementation of such type of integrated circuit [9].

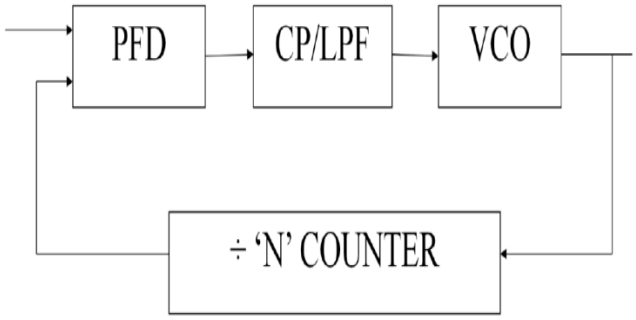

Fig. 1: Basic block diagram of a PLL

A PLL is a negative feedback control system circuit. As the name implies, the purpose of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is done after many iterations of comparing the reference and feedback signals.

The overall goal of the PLL is to match the reference and feedback signals in phase, this is the lock mode. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

A basic form of a PLL consists of five main blocks:
1.Phase Frequency Detector (PFD) 2. Charge Pump (CP) 3. Low Pass Filter (LPF) 4. Voltage Controlled Oscillator (VCO) 5. Frequency Divider.
Some applications of Phase locked loop are:

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1. Frequency Synthesis
2. Clock Generation
3. Carrier Recovery (Clock Recovery)
4. Skew Reduction
5. Jitter and Noise Reduction

A. PHASE FREQUENCY DETECTOR

The Phase frequency Detector (PFD) is one of the main part in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals "UP" and "DOWN". Fig. 2 shows a traditional PFD circuit.

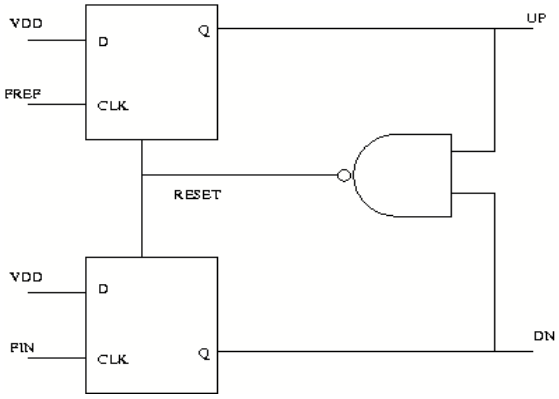

Fig. 2: Block Diagram of PFD using NAND gate

B. CHARGE PUMP

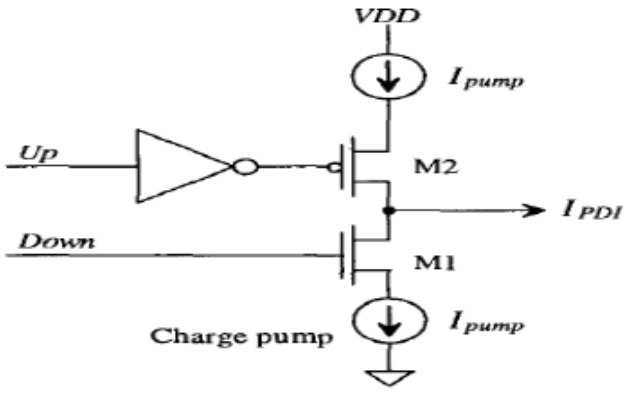

Fig. 3: Block Diagram of Charge Pump

The fig. 3 shows the schematic of Charge Pump. The operation of circuit is as follows. When the UP signal goes high M2 transistor turns ON while M1 is OFF and the output current is IPDI with a positive polarity. When the down signal becomes high M1 transistor turns ON while M2 is OFF and the output current is IPDI with a negative polarity [3].

C.LOOP FILTER

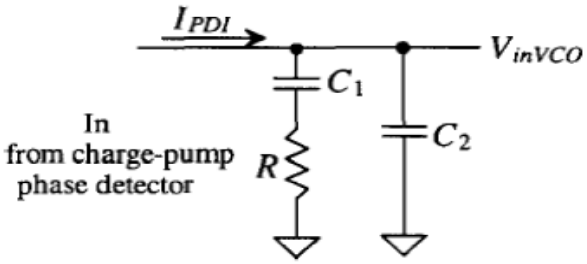

Fig. 4: Block Diagram of Loop Filter

The passive low pass loop filter is used to convert back the charge pump current into the voltage. The filter should be as compact as possible [3].The output voltage of the loop filter controls the oscillation frequency of the VCO. The loop filter voltage will increase if Fref rising edge leads Fin rising edge and will decrease if Fin rising edge leads Fref rising edge. If the PLL is in locked state it maintains a constant value.

D.VOLTAGE CONTROLLED OSCILLATOR

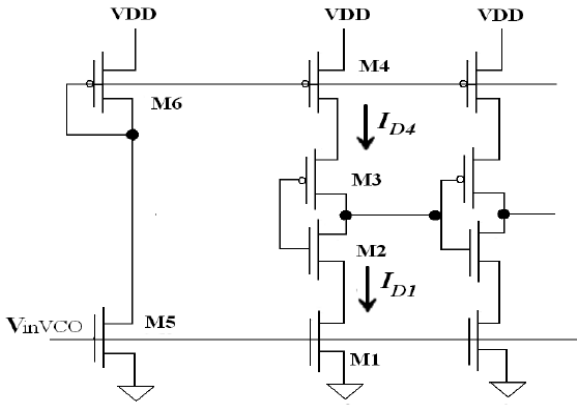

Fig. 5: Block Diagram of Voltage Controlled Oscillator

An oscillator is an autonomous system which generates a periodic output without any input. The most popular type of the VCO circuit is the current starved voltage controlled oscillator (CSVCO). Here the number of inverter stages is fixed with 5. The simplified view of a single stage current starved oscillator is shown in the Fig. 5 [3] [5].

E. FREQUENCY DIVIDER

The output of the VCO is fed back to the input of PFD through the frequency divider circuit. The frequency divider in the PLL circuit forms a closed loop. It scales down the frequency of the VCO output signal. A simple D flip flop (DFF) acts as a frequency divider circuit. The schematic of a simple DFF based divide by 2 frequency divider circuit is shown in the Fig. 6.

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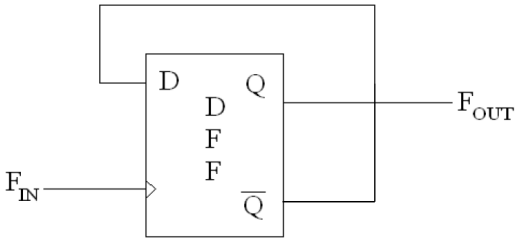

Fig. 6: Block Diagram of Frequency Divider

III. SIMULATION RESULTS AND WAVEFORMS

The Pass Transistor DFF PFD circuit is shown in Fig.7 [4]. The PFD is same as to a dynamic two-phase master-slave pass-transistor flip-flop. The clock skew is minimized by using single edge clocks.

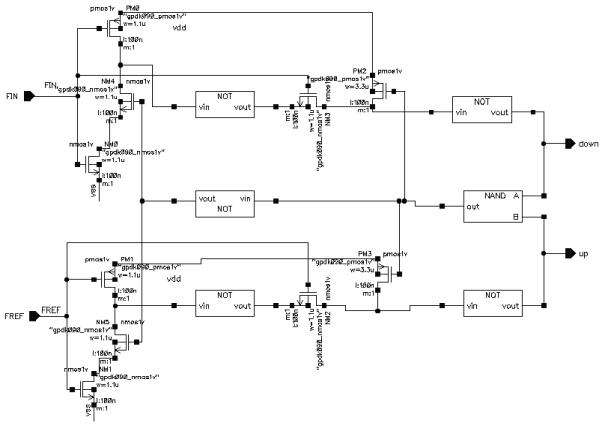

Fig. 7: Schematic of Phase Frequency Detector

The PFD circuit can be analyzed in three different ways. One way, in which FREF leads FIN, second way in which FREF lags FIN, the other in which FREF and FINS same.

The output of the PFD when FREF signal rising edge leads FIN signal rising edge and vice versa is shown in the Figure 8 and Fig. 9 respectively. Fig. 10 shows when FREF signal rising edge same as FIN signal rising edge.

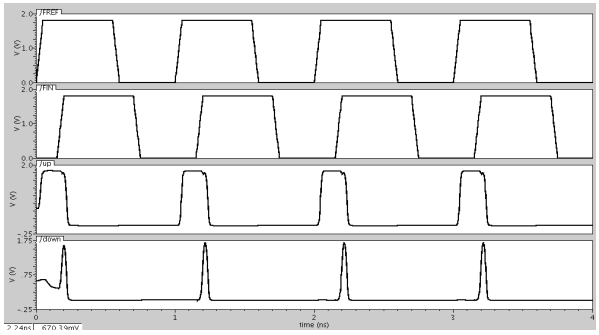

Fig. 8: Simulation Result of PFD(when Fref leads Fin)

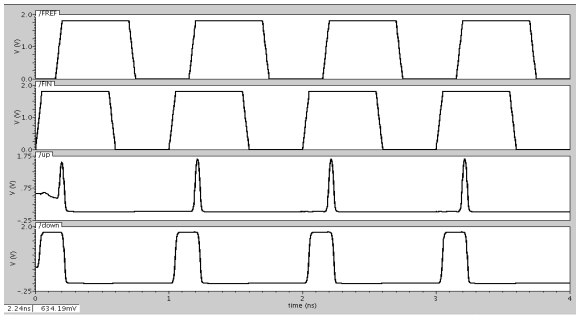

Fig. 9: Simulation Result of PFD(when Fref lags Fin)

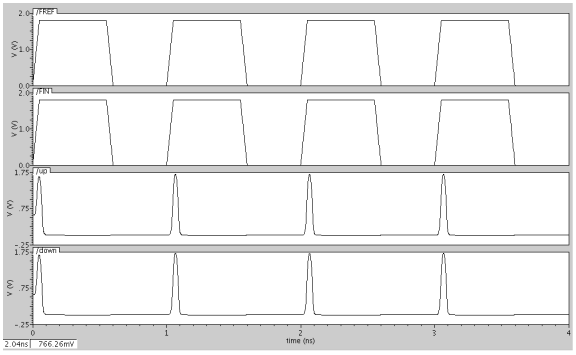

Fig. 10: Simulation Result of PFD(when Fref & Fin are same)

The Schematic of Charge Pump is shown in Fig.11.The output of the PFD should be combined into a single output for driving the loop filter. When the PFD up signal goes high, PMOS turns on, connecting the current source to the loop filter. Since the current source can be made insensitive to supply variation, modulation of VCO control voltage is absent. In order to adjust the delay between up and down, a complimentary pass gate is added into the circuit between down and the upper NMOS.

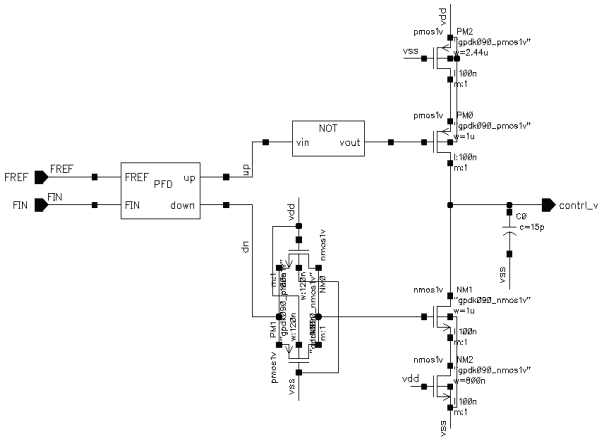

Fig. 11: Schematic of Charge Pump

Fig. 12 and Fig. 13 shows simulation results of Charge Pump while charging and discharging respectively.

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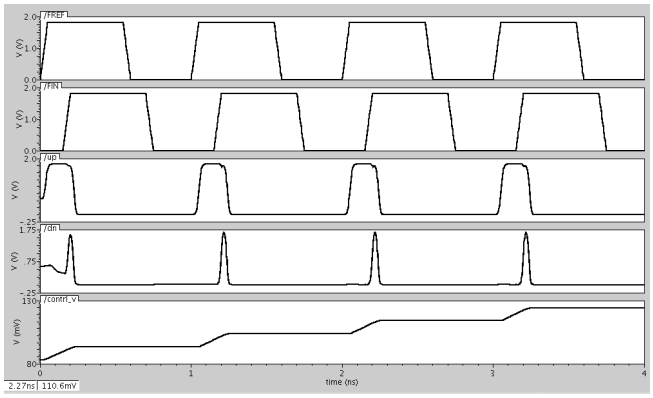

Fig. 12: Simulation of Charge Pump (When Charging)

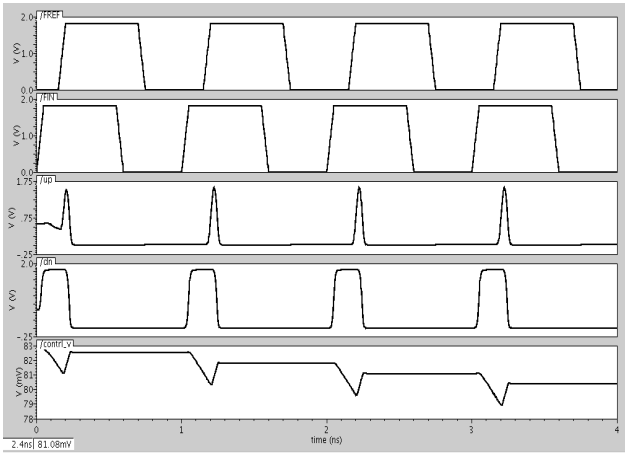

Fig. 13: Simulation of Charge Pump (When Charging)

The loop filter is the brain of PLL. If the loop filter values are not selected correctly, it may take the loop too long to lock, or once locked small variations in the input data may cause the loop to unlock. Fig.14 shows schematic of loop filter. The value of C2 is about one-fifth to one tenth of C1.

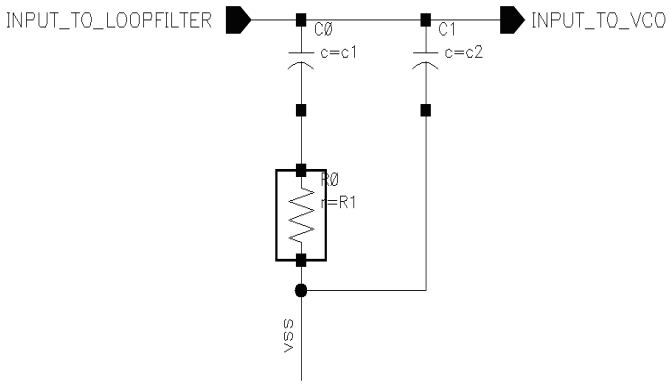

Fig. 14: Schematic of Loop Filter

The heart of the PLL circuit is the voltage controlled oscillator. Fig. 15 shows schematic of current starved voltage controlled oscillator. The circuit is designed to give a center frequency of oscillation of 1 GHz. The center frequency of an oscillation at input control voltage of VDD/2 is 1.05 GHz. The output signal of the VCO at a control voltage of VDD/2 is shown in the Fig.16. Fig. 17 shows VCO charactestics curve.

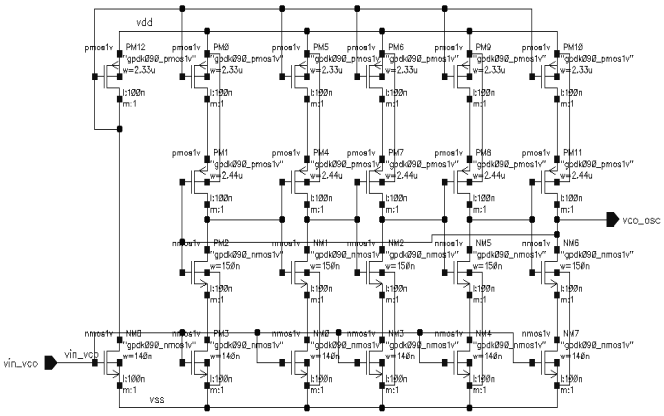

Fig. 15: Schematic of Current Starved VCO

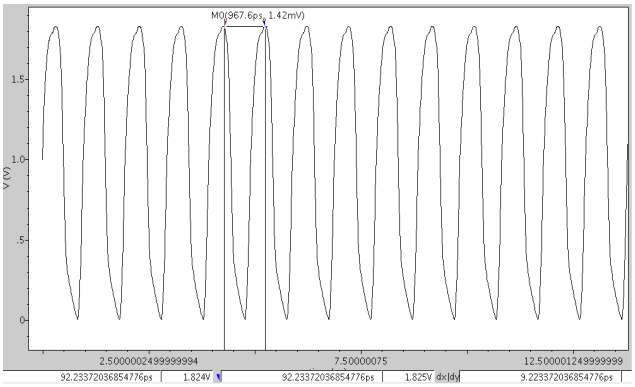

Fig. 16: Schematic of Current Starved VCO

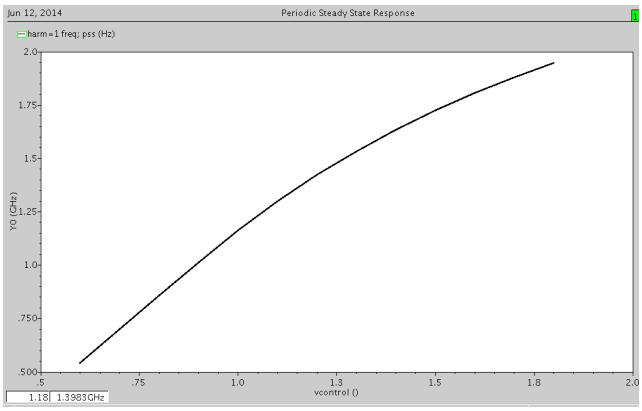

Fig. 17: VCO characteristics curve

The circuit diagram of a pass transistor based DFF frequency divider circuit is shown in the Fig. 18. The circuit divides the

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frequency by a factor of 2. The simulation result of the divide by 2 circuits is shown in the Fig. 19.

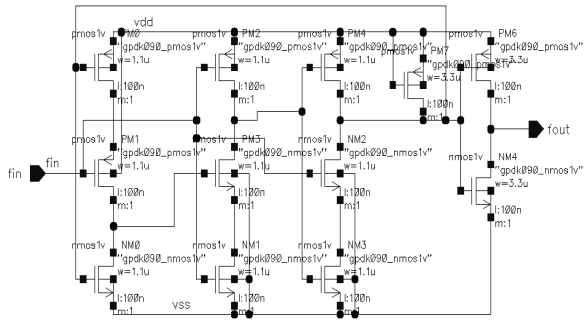

Fig. 18: Schematic of Frequency Divider

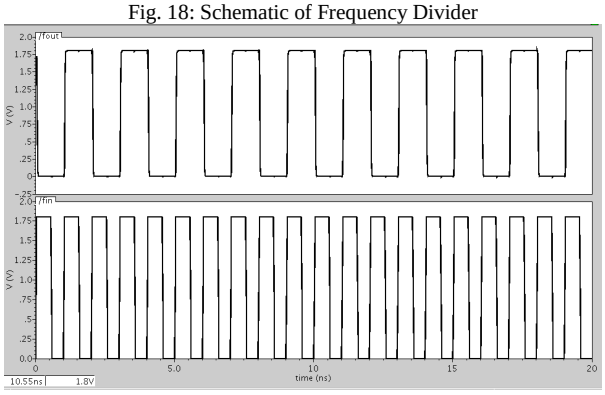

Fig. 19: Simulation of Frequency Divider

Fig. 20 shows schematic of PLL.The output of the charge pump and loop filter circuit i.e. the control voltage will maintain a constant value when the references signal and feed-back signal are in lock.

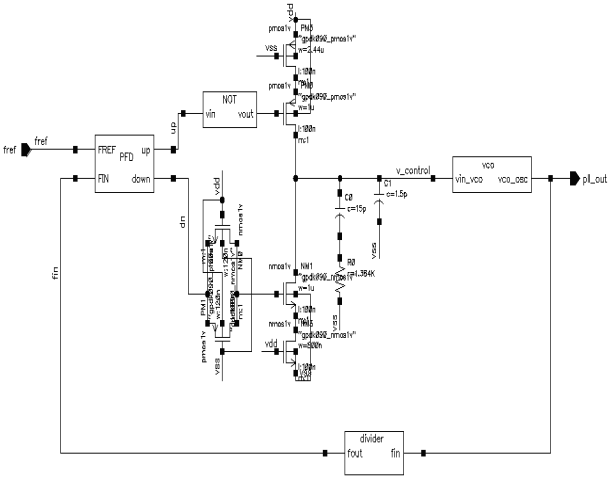

Fig. 20: Schematic of PLL

Different signals like UP, DOWN, Control Voltage, reference signal and feedback input signal of the PLL in the lock state are shown in the Figure21 and from Figure21 its clear that when the control voltage is constant, the reference signal and the feedback input signal are almost similar as their phase and frequency are approximately same.

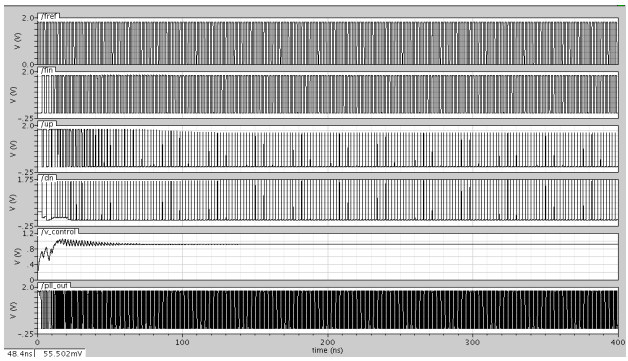

Fig. 21: Simulation of PLL

The control voltage of PLL for the schematic level is shown in the Fig. 22. From the Fig. 22 it's clear that the control maintains the constant value of 0.9 V at time 100 ns. So the lock time of PLL is 100 ns.

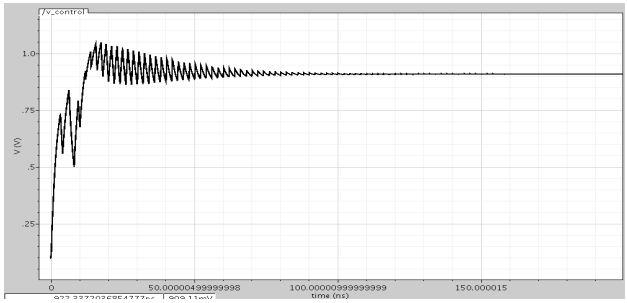

Fig. 22: Control Voltage of VCO

Table 1: Simulation Parameters of PLL

Parameter	Result of Current Work	Results reported in [10]	Results reported in [8]
Technology	90 nm	90nm	180nm
Supply voltage	1.8V	1.8V	5V
Average Current	482.5 uA	-	-
Maximum Power Consumption	868.5 uW	11.9mW	-
Lock Time	100 ns	280.6ns	643.358ns
Frequency	1 GHz	1 GHz	1 GHz
Phase Noise -	-	54.12dBc/Hz	-

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Table 2: Simulation Parameters of PLL Lock time, Average Current, Total Power dissipation for different process corners (vdd=1.8V) (Temp=27°C).

Process Corners	Lock time	Average Current (uA)	Power Consumption (uW)
Typical(NN)	100n	482.5	868.5
Slow Slow(SS)	110n	404.4	727.92
Slow Fast(SF)	50n	682.1	1227.78
Fast Slow(FS)	70n	472.9	851.22
Fast Fast(FF)	80n	511.0	919.8

Table 3: Lock time, Average Current, Total Power dissipation at different Temperatures (vdd=1.8V) Process Corners Typical (NN).

Temperature (degree Celsius)	Lock time (ns)	Average Current (uA)	Power consumption (uW)
-50	90	493	887.4
-40	93	486	874.8
-30	94	484	871.2
-20	95	487	876.6
-10	96	485	873
0	97	484.7	872.4
10	98	481.3	866.3
20	99	481.8	867.2
30	100	482.8	869.0
40	98	480.7	865.2
50	97	482	867.6
60	96	486	874.8
70	94	490	882
80	90	492.8	887.04
90	88	498.7	897.6
100	80	500	900

CONCLUSION

Minimization of power consumption is essential for high performance VLSI systems. The lock time of the PLL mainly depends upon the type of PFD architecture used and the parameters of the charge pump and loop filter. So by properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values a better lock time can be achieved. In this work a PLL with a better lock time is presented. The lock time of the PLL is found to be 100 ns. The PLL circuit consumes a power of 867 uW from a 1.8 V D.C. supply.

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