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Design of high speed, Low area 32 bit MAC Unit using Vedic Multiplier

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***Abstract*— This paper presents Multiply and Accumulate (MAC) unit design using Vedic Multiplier, which is based on Urdhva Tiryagbhyam Sutra. The paper emphasizes an efficient 32-bit MAC architecture along with 16-bit version and results are presented in comparison with conventional architectures. The efficiency in terms of area and speed of proposed MAC unit architecture is observed through reduced area, low critical delay and low hardware complexity. Comparison is made with the delay of MAC with different FPGA technology in Xilinx. The Simulation is performed using ISE and power analysis is done using the Xilinx tool for synthesis. The implemented architecture shows the improvement in delay and the low area is obtained based on the performance**

Index Terms— **Vedic Mathematics, urdhva triyakbhyam sutra, vedic multiplier.**

I INTRODUCTION

The general MAC architecture consists of a conventional multiplier, adder and an accumulator. Where the output is added to the previous MAC output result by an accumulate adder. The Multiply-Accumulate (MAC) unit is extensively used in microprocessors and digital signal processors for data-intensive applications, such as filtering, convolution, and inner products. Most digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transform (DWT) or FFT/IFFT computations that can be efficiently accelerated by dedicated MAC units. Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition determines the execution speed and performance of the entire computation. As the multiplier exhibits inherently long delay among the basic operational blocks in digital system, the multiplier determines the critical path.

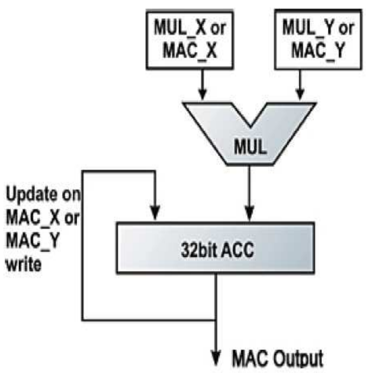

Fig. 1 Block diagram of MAC unit with Vedic multiplier.

II VEDIC MAC UNIT

Multiply and Accumulate (MAC) unit design using Vedic Multiplier, which is based on Urdhva Tiryagbhyam Sutra. The paper emphasizes an efficient 32-bit MAC architecture along with 16-bit version and results are presented in comparison with conventional architectures. The efficiency in terms of area and speed of proposed MAC unit architecture is observed through reduced area, low critical delay and low hardware complexity. The proposed MAC unit reduces the area by using MUX in multiplier which uses two multipliers Instead of four multipliers and from reducing the number of multipliers and Units Increase in the speed of operation is achieved by the hierarchical nature of the Vedic multiplier unit. The proposed MAC unit is implemented on a field programmable gate array (FPGA) device, 3S100ETQ144-5 (Spartan 3). The performance evolution

results in terms of speed and device utilization are compared to earlier MAC architecture. Though the use of Vedic mathematics methods for multiplication is reported in literature, it has been observed that our proposed method of 32-bit MAC unit implementation is using (32X32) multiplication unit and shows improvements in the delay and area.

III VEDIC MULTIPLIER

Proposed Algorithm:

From ancient Vedic mathematics Urdhva Tiryagbhyam Sutra is used in all general multiplication and it literally means "vertically and crosswise". Urdhva-tiryagbhyam sutra of width NXN will generate the 2N-1 cross products of different widths which when combined forms (log2N + 1) partial products. The partial products are obtained by vertical and crosswise operations.

Urdhav Triyakbhtam logic shown in the figure 2 .a shows how two 4-bit numbers are multiplied. Multiplication starts from the LSB bit of the numbers as shown

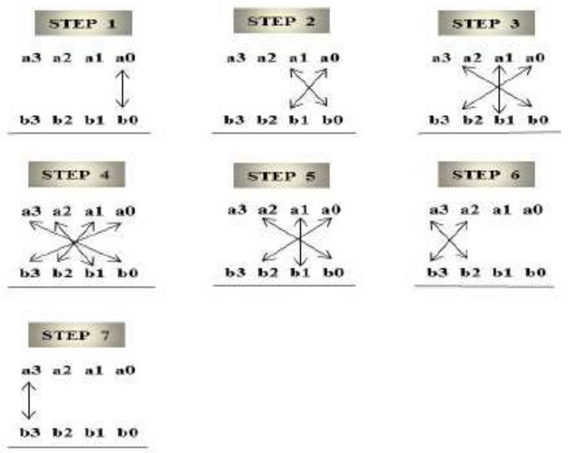

Fig 2 Multiplication of 4 bit numbers using urdhva triyakbhyam

1.2x2 Vedic Multiplier

In this the hardware realisation of 2x2 bit Vedic multiplier is used in the figure given below .In this clock and registers are not used for the sake of simplicity. But the emphasis is laid on the understanding of the algorithm.

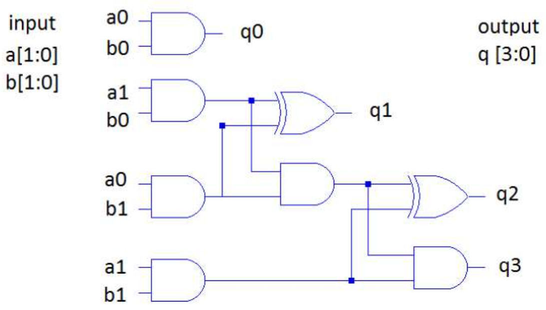

Fig. 3. 2 -Bit Vedic multiplier.

2.4x4 Vedic Multiplier

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In this 4x4bit multiplier is made by using 4,2x2 multiplier blocks here multiplicands are of bit size(n=4) where as the result of 8bit size .The input is broken into smaller chunks of size n?2,for both inputs, that is a and b. These newly formed chunks of 2bits are given as input into 2x2 multiplier and the result produced 4bit,which are the output produced from 2x2 multiplier blocks are sent for addition to an addition tree.

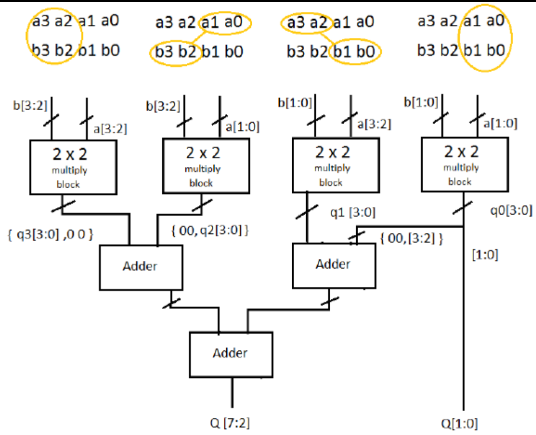

Fig. 4. 4- Bit Vedic multiplier.

And the same way the designing of 32x32 bit is done.

IV RESULTS AND ANALYSIS

The simulation is done using the ISE version for 16 bit and 32 bit and power analysis is performed using the XILINX 13.1 version.

DESIGN : XCS100E
PACKAGE : TQ144
SPEED : -5
OPTIMIZATION GOAL : SPEED
LUT COMBINING : NO

There is an improved performance like less delay and power with different technologies of FPGA's.

Table 1.Delay comparison with different family of FPGA with improvement in proposed architecture's result

No. of bits	Parameter	Device Spartan 2S200PQ 208[2]	Device Spartan 3S100ET Q144-5[1]	Device Spartan 3S100ET Q144-5
16	Delay(ns)	22.604	10.213	7.283
32	Delay(ns)	35.76	14.69	9.495

Table 2.Area Utilization Report of MAC

size	Slice logic utilization	Used resources	Utilization %
16 bit	Number of Slice LUTs	186 of 960	19%
16 bit	Number of 4 input LUTS	348 of 1920	18%
32 bit	Number of Slice LUTs	224 0f 960	23%
32 bit	Number Of 4 input LUTS	447 of 1920	23%

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The simulated result is shown below using MODELSIM for 16 bit and 32- bit.

Simulated waveforms for 16 bit:

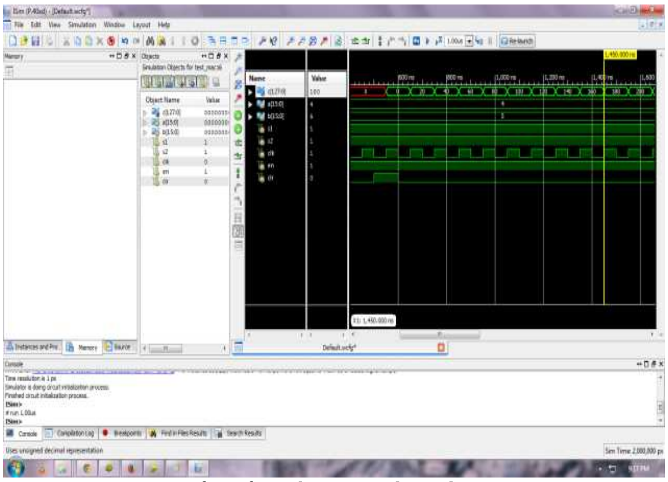

Fig 4.Waveform from the RTL code -16 bit MAC Unit

In the above simulation a= 4and b=5 in decimal and the MAC output c=20,40 and etc is obtained.

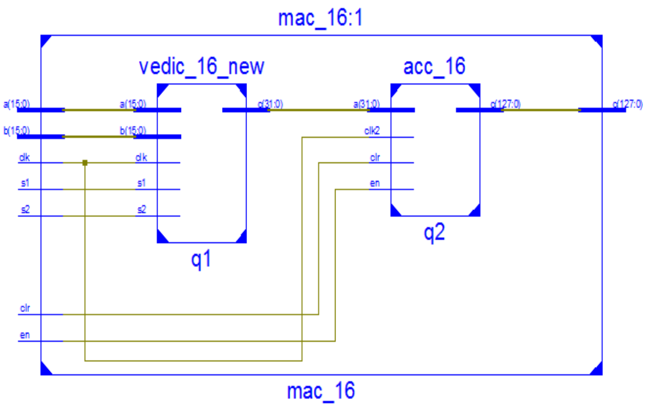

Fig 5.RTL schematic for 16-bit MAC using Mux. Simulated waveforms for 32-bit:

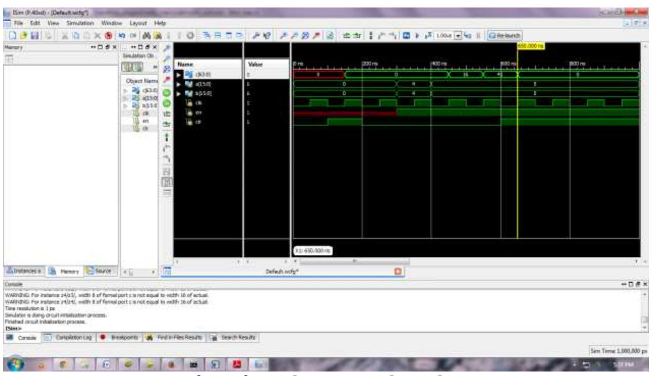

Fig 6.Waveform from the RTL code 32-bit MAC Unit

In the above simulation a=4,5 and b=4,5 in decimal and the MAC output c=16,41 is obtained.

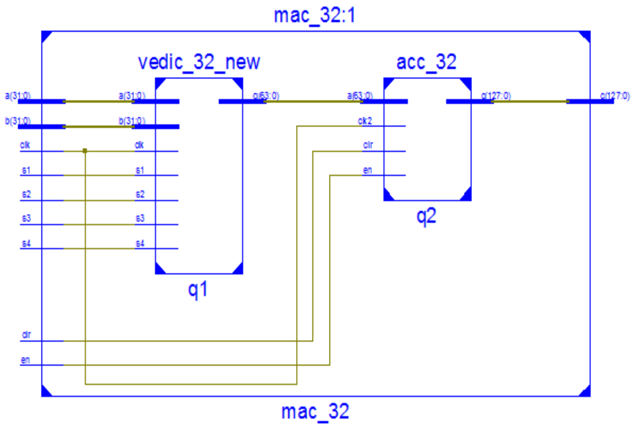

Fig 6.Waveform from the RTL code 32-bit MAC Unit

VI CONCLUSION

An efficient MAC unit using Vedic multiplier is designed and implemented. Its performance and delay has been estimated with the speed optimization. The Mac unit is compared with various FPGA families and delay report for 16 and 32bit has been tabulated.

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REFERENCE

[1]. Ramalatha, M.Dayalan, K D Dharani, P Priya, and S Deoborah, High Speed Energy Efficient ALU design using Vedic multiplication techniques, International Conference on Advances in Computational Tools for Engineering Applications, 2009. ACTEA ’09.pp. 600-3, Jul 15-17, 2009.

[2]. Sree Nivas A and Kayalvizhi N. Article: Implementation of Power Efficient Vedic Multiplier. International Journal of Computer Applications 43(16):21-24, April 2012. Published by Foundation of Computer Science, New York, USA .

[3]. Modified Architecture of Vedic Multiplier for High Speed Applications- International Journal of Engineering Research & Technology (IJERT),Vol. 1 Issue 6, August – 2012. 4. Low Power ALU Design by Ancient Mathematics- 2010 IEEE.

[4]. Vedic Mathematics Based 32-Bit Multiplier Design for High Speed Low Power Processors-INTERNATIONAL JOURNAL ON SMART SENSING AND INTELLIGENT SYSTEMS VOL. 4, NO. 2, JUNE 2011 268.

[5]. Design of high speed Vedic multiplier using Vedic mathematics techniques, G.Ganesh Kumar, V.Charishma - International Journal of Scientific and Research Publications, Volume 2, Issue 3, March, 2012.

[6]. Compare Vedic Multipliers with Conventional Hierarchical array of array multiplier-International Journal of Computer Technology and Electronics Engineering (IJCTEE)Volume 2, Issue 6.

[7]. Vedic Mathematics for Fast Multiplication in DSP-International Journal of Engineering and Innovative Technology (IJEIT)Volume 2, Issue 8, February 2013.