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Seven Level Switched-Capacitor Inverter Using Multilevel Conversion with Inductive Load

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Abstract: **Recently, electricity systems, electrical vehicles (EVs), and distributed generation (DG) systems, etc., area unit centered thanks to the world environmental problems. The ability physical science, converters and inverters, may be a key technology in these systems. A switched-capacitor (SC) electrical converter outputs structure voltages with switched capacitors. Associate SC electrical converter is comparable to a charge pump within the topology. The SC electrical converter outputs a bigger voltage than the input voltage in similar thanks to the charge pump. However, the SC electrical converter additionally has several shift devices that create the system sophisticated. On the opposite hand, a Marx electrical converter, that has less shift devices compared to the SC electrical converter, was projected. Marx electrical converter are often considered one in every of the SC inverters thanks to its operation principle. In this paper, the circuit configuration, the theoretical operation, the simulation results with MATLAB/SIMULINK, and also the experimental results area unit shown. The experimental results accorded with the theoretical calculation and also the simulation results.**

Keywords**: Inverter, SC, SDCS, H-Bridges, PWM, PDPWM, DG**

1. INTRODUCTION

The EVs and also the grid connected decigram systems want Associate in nursing electrical converter to convert dc to ac. Boost converters or transformers square measure wide utilized in these systems once the input voltage is smaller than the output voltage. However, an electrical device or Associate in nursing electrical device within the boost device makes the system giant, as a result of the electrical device and also the electrical device should have giant and significant magnetic cores to sustain the high power. As a provision against the problem, a charge pump, that doesn't have any inductors, is applied to such systems.

A charge pump outputs a bigger voltage than the input voltage with switched capacitors. Once the many capacitors and also the input voltage sources square measure connected in parallel, the capacitors square measure charged. Once the many capacitors and also the input voltage sources square measure connected asynchronous, the capacitors square measure discharged. The charge pump outputs the add of the voltages of the capacitors and also the input voltage sources. However, a charge pump has several switch devices that create the system a lot of difficult.

In this paper, Associate in Nursing SC electrical converter whose structure is less complicated than the traditional SC electrical converter is planned. It consists of a Marx electrical converter structure Associate in Nursing an H-bridge. The planned electrical converter will output larger voltage than the input voltage by switch the capacitors asynchronous and in parallel. The planned electrical converter doesn't have any inductors that create the system giant. The output harmonics of the planned electrical converter square measure reduced by the construction output.

2. MULTILEVEL CONVERTER

Inverter: An inverter is an electrical device that converts direct current (DC) to alternating current (AC); the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high-voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. The electrical inverter is a high-power electronic oscillator. It is so named because early mechanical AC to DC converters was made to work in reverse, and thus was "inverted", to convert DC to AC. The inverter performs the opposite function of a rectifier

Cascaded H-Bridges Inverter: A single-phase structure of an m-level cascaded inverter is illustrated in Figure. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge

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inverter with 5 SDCSs and 5 full bridges is shown in Figure 31.2. The phase voltage $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$.

For a stepped waveform such as the one depicted in Figure 31.2 with s steps, the Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sum_{n}\left[\cos(n\theta_1)+\cos(n\theta_2)+\ldots+\cos(n\theta_s)\right]\frac{\sin(n\omega t)}{n}, \quad \text{where } n = 1, 3, 5, 7, \ldots$$

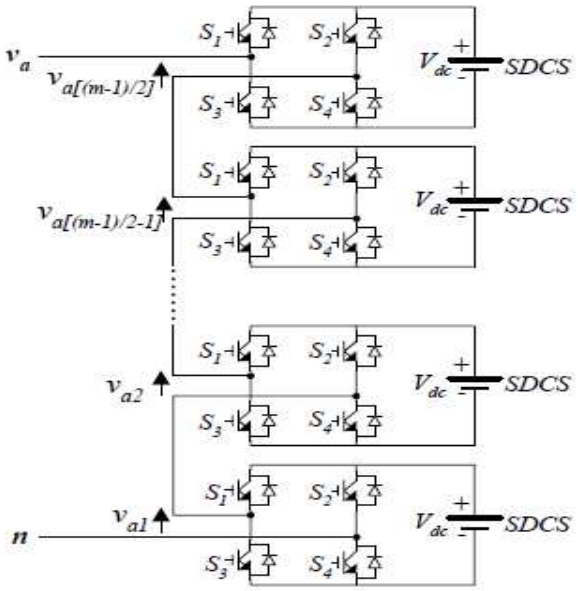

Fig.1. Single-phase structure of a multilevel cascaded H-bridges inverter

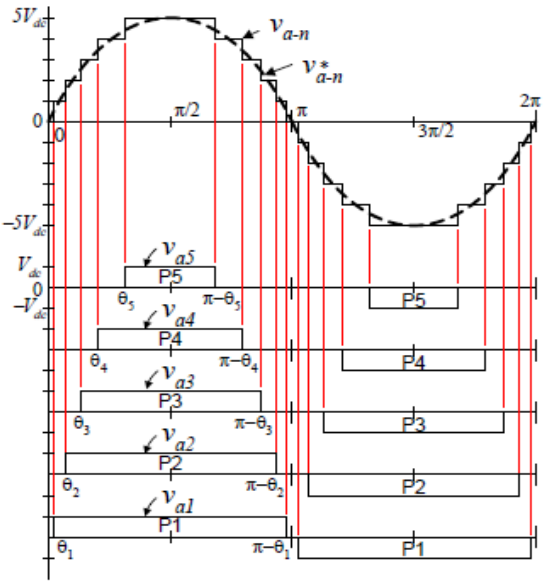

Fig.2. Output phase voltage waveform of an 11-level cascade inverter with 5 separate dc sources.

The magnitudes of the Fourier coefficients when normalized with respect to V_{dc} are as follows:

$$H(n) = \frac{4}{\pi n}\left[\cos(n\theta_1)+\cos(n\theta_2)+\ldots+\cos(n\theta_s)\right], \quad \text{where } n$$

The conducting angles, θ_1, θ_2,... θ_s, can be chosen such that the voltage total harmonic distortion is a minimum. Generally, these angles are chosen so that predominant lower frequency harmonics, 5th, 7th, 11th, and 13th, harmonics are eliminated. More detail on harmonic elimination techniques will be presented in the next section.

Multilevel cascaded inverters have been proposed for such applications as static var generation, an interface with renewable energy sources, and for battery-based applications. Three-phase cascaded inverters can be connected, as shown in Figure, or in delta. A prototype multilevel cascaded static var generator connected in parallel with the electrical system that could supply or draw reactive current from an electrical system.

The inverter could be controlled to either regulate the power factor of the current drawn from the source or the bus voltage of the electrical system where the inverter was connected. A cascade inverter can be directly connected in series with the electrical system for static var compensation. Cascaded inverters are ideal for connecting renewable energy sources with an ac grid, because of the need for separate dc sources, which is the case in applications such as photovoltaic's or fuel cells.

Cascaded inverters have also been proposed for use as the main traction drive in electric vehicles, where several batteries or ultra capacitors are well suited to serve as SDCSs. The cascaded inverter could also serve as a rectifier/charger for the batteries of an electric vehicle while the vehicle was connected to an ac supply as shown in Figure. Additionally, the cascade inverter can act as a rectifier in a vehicle that uses regenerative braking.

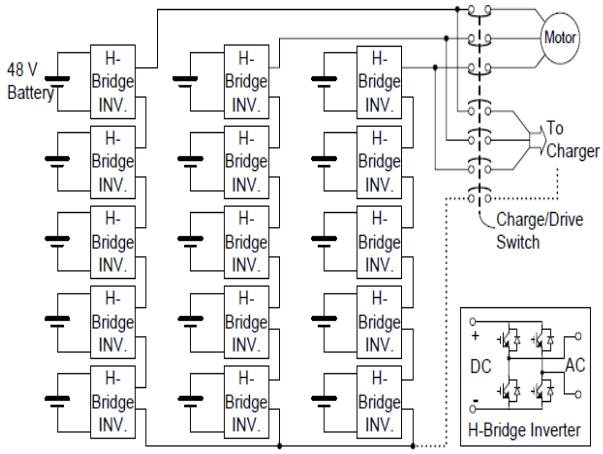

Fig.3. Three-phase connection structure for electric vehicle motor drive and battery charging.

The main advantages and disadvantages of multilevel cascaded H-bridge converters are as follows

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3. MULTICARRIER PWM SCHEMES:

In this section four different control techniques as well as the proposed control scheme are discussed.

A. Phase Shifted PWM

The essential principle of PSPWM is phase shifting the carriers of each bridge to achieve additional harmonic sideband cancellation, which occur around the even carrier multiple groups. Fig. 3 shows the carrier arrangements for the three H-bridge cells connected in series in one of the phase legs of a seven level-cascaded structure. Optimum harmonic cancellation is achieved by phase shifting each carrier by (k-1) /n, where k is the k th converter, n is the number of series-connected single-phase inverters per phase leg. For three cascaded H-bridges with the carrier phase shift of 60°, harmonic cancellation up to side bands around multiples of 6fc will be achieved. The cancellation is not dependent on the carrier/fundamental frequency ratio.

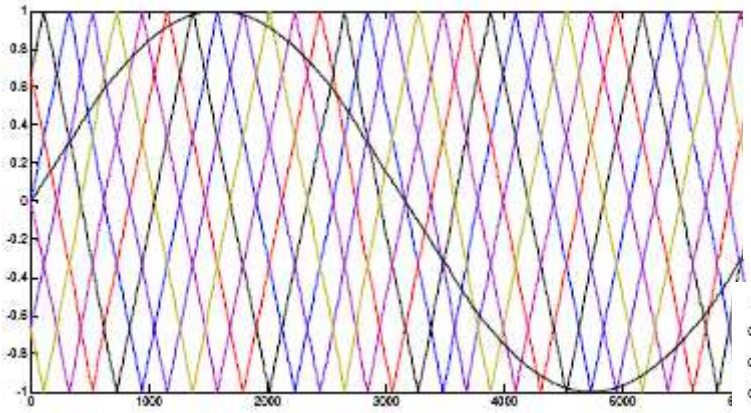

Fig.4. PSPWM Technique

B. Carrier Disposition PWM

In this carrier disposition PWM (CDPWM) method modulation is achieved by having L-1 triangular carriers where L is the number of voltage levels. These carriers are arranged so that they fully occupy continuous bands in the range of -(L-1) Vdc/2 to (L-1) V_{dc}/2 (for L odd). A single sinusoidal reference is then compared with these carriers to determine the switched voltage level. The degree of freedom for these CDPWM techniques is given as:

$$M_a = \frac{2 \times A_r}{(L-1) \times A_c} \qquad (1)$$

Where, *Ar* is the amplitude of the reference waveform. *Ac* is the amplitude of the carrier waveform. *L* is the number of levels.

This CDPWM strategy includes phase disposition pulse width modulation (PDPWM), phase opposition disposition pulse width modulation (PODPWM) and alternative phase opposition disposition (APODPWM). In the PDPWM technique all the carriers are in phase across all the bands as described in Fig. 4. The PODPWM is explained in the Fig. 5, in which all the carriers above the zero reference are in phase and carriers below the zero reference are also in phase but are phase shifted by 180° with respect to that above zero reference. But in APODPWM carriers in adjacent bands are phase displaced by 180°, which is shown in Fig. .

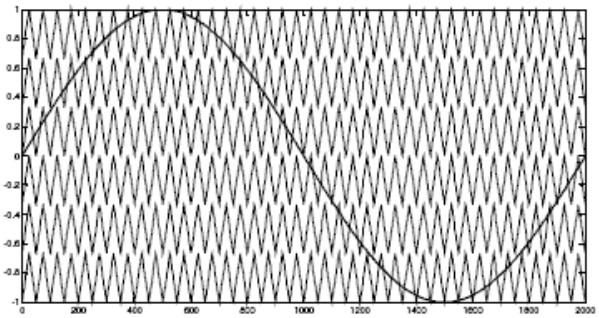

Fig.5. PDPWM technique for 3-cell Bridge

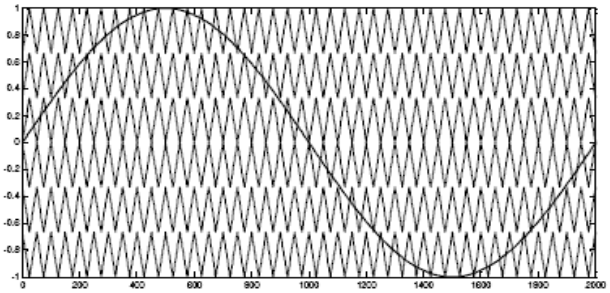

Fig.6. PODPWM Technique for 3-cell H-Bridge Inverter

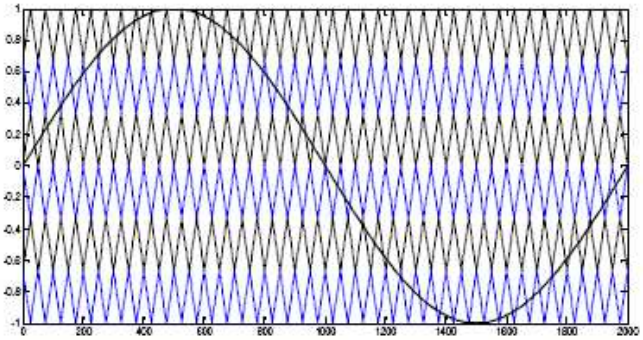

Fig.7. APODPWM Technique for 3-cell H-Bridge Inverter

4. SWITCHED CAPACITOR (SC)

A switched capacitor is an electronic circuit element used for discrete time signal processing. It works by moving charges into and out of capacitors when switches are opened and closed. Usually, non-overlapping signals are used to control the switches, so that not all switches are closed simultaneously. Filters implemented with these elements are termed "switched-capacitor filters," and depend only on the ratios between capacitances. This makes them much more suitable for use within integrated circuits, where accurately specified resistors and capacitors are economical to construct. The switched capacitor resistor the simplest switched capacitor (SC) circuit is the switched capacitor resistor, made

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of one capacitor C and two switches S_1 and S_2 which connect the capacitor with a given frequency alternately to the input and output of the SC. Each switching cycle transfers a charge q from the input to the output at the switching frequency f. Recall that the charge q on a capacitor C with a voltage V between the plates is given by:

$$q = CV$$

where V is the voltage across the capacitor. Therefore, when S_1 is closed while S_2 is open, the charge stored in the capacitor C_S is:

$$q_{\mathrm{IN}} = C_S V_{\mathrm{IN}}.$$

When S_2 is closed, some of that charge is transferred out of the capacitor, after which the charge that remains in capacitor C_S is:

$$q_{\mathrm{OUT}} = C_S V_{\mathrm{OUT}}.$$

Thus, the charge moved out of the capacitor to the output is:

$$q = q_{\mathrm{IN}} - q_{\mathrm{OUT}} = C_S(V_{\mathrm{IN}} - V_{\mathrm{OUT}})$$

Because this charge q is transferred at a rate f, the rate of transfer of charge per unit time is:

$$I = qf.$$

Note that we use I, the symbol for electric current, for this quantity. This is to demonstrate that a continuous transfer of charge from one node to another is equivalent to a current. Substituting for q in the above, we have:

$$I = C_S(V_{\mathrm{IN}} - V_{\mathrm{OUT}})f$$

Let V be the voltage across the SC from input to output. So:

$$V = V_{\mathrm{IN}} - V_{\mathrm{OUT}}.$$

So the equivalent resistance R (i.e., the voltage–current relationship) is:

$$R = \frac{V}{I} = \frac{1}{C_S f}.$$

Thus, the SC behaves like a lossless resistor whose value depends on capacitance C_S and switching frequency f. The SC resistor is used as a replacement for simple resistors in integrated circuits because it is easier to fabricate reliably with a wide range of values. It also has the benefit that its value can be adjusted by changing the switching frequency (i.e., it is a programmable resistance). See also: operational amplifier applications. $q = CV$ This same circuit can be used in discrete time systems (such as analog to digital converters) as a track and hold circuit. During the appropriate clock phase, the capacitor samples the analog voltage through switch one and in the second phase presents this held sampled value to an electronic circuit for processing.

Determination of Capacitance

The capacitance C_k can be determined properly with considering the voltage ripple of the capacitors C_k. The smaller voltage ripple of these capacitors leads to the higher efficiency.

In this section, the capacitance C_k are calculated when the maximum voltage ripple is supposed to be 10% of the maximum voltages of the capacitors.

The capacitors C_k are charged when they are connected in parallel and are discharged when they are connected in series. From Fig. 3, the switches S_{a1} and S_{a2} of the proposed inverter (n = 2) are symmetrically driven during the half cycle of the reference waveform. Therefore, the voltage ripple of the capacitor $C1$ is focused.

Assuming that the power factor of the output load cosφ = 1, the longest discharging term of the capacitor $C1$ in the proposed inverter (n = 2) is between t2 and t3 in Fig. 3. Assuming the modulation index M = 3, the time t_1, t_2 and t_3 in Fig. 3 are

$$t_1 = \frac{\sin^{-1}(1/3)}{2\pi f_{ref}} \quad (4)$$

$$t_2 = \frac{\sin^{-1}(2/3)}{2\pi f_{ref}} \quad (5)$$

$$t_3 = \frac{\pi - \sin^{-1}(2/3)}{2\pi f_{ref}} \quad (6)$$

Where f_{ref} is the frequency of the reference waveform. Therefore, the maximum discharge amount Q_1 of the capacitor C_1 is

$$Q_1 = \int_{t_2}^{t_3} I_{bus} \sin(2\pi f_{ref} t - \phi)\, dt \quad (7)$$

Where I_{bus} is the amplitude of the bus current waveform and φ is the phase difference between the bus voltage waveform v_{bus} and the bus current waveform i_{bus}. Q_1 supposes to be less than 10% of the maximum charge of C_1. Therefore, the capacitance C_1 must satisfy

$$C_1 > \frac{Q_1}{0.1V_{in}} \quad (8)$$

When the capacitors C_k satisfy (8), the other voltage ripple which is caused by PWM is less than 10%. The peak current of the capacitor I_{C1} is calculated by

$$I_{C1} = \frac{V_{in} - V_{C1}}{r_{c1} + 2r_{on}} \quad (9)$$

Where r_{c1} is the equivalent series resistance (ESR) of the capacitor C_1 and r_{on} is the internal resistance of the switching devices. From (9), the peak current of the capacitor C_1 is determined by the difference between the input voltage V_{in} and the voltage of the capacitor V_{C1}, and the internal resistance of the switching devices. The difference of the voltages $V_{in} - V_{C1}$ is small when the capacitance C_1 is large. Therefore, when the switches which have small internal resistance are used, the capacitance $C1$ must be larger to prevent the large peak current.

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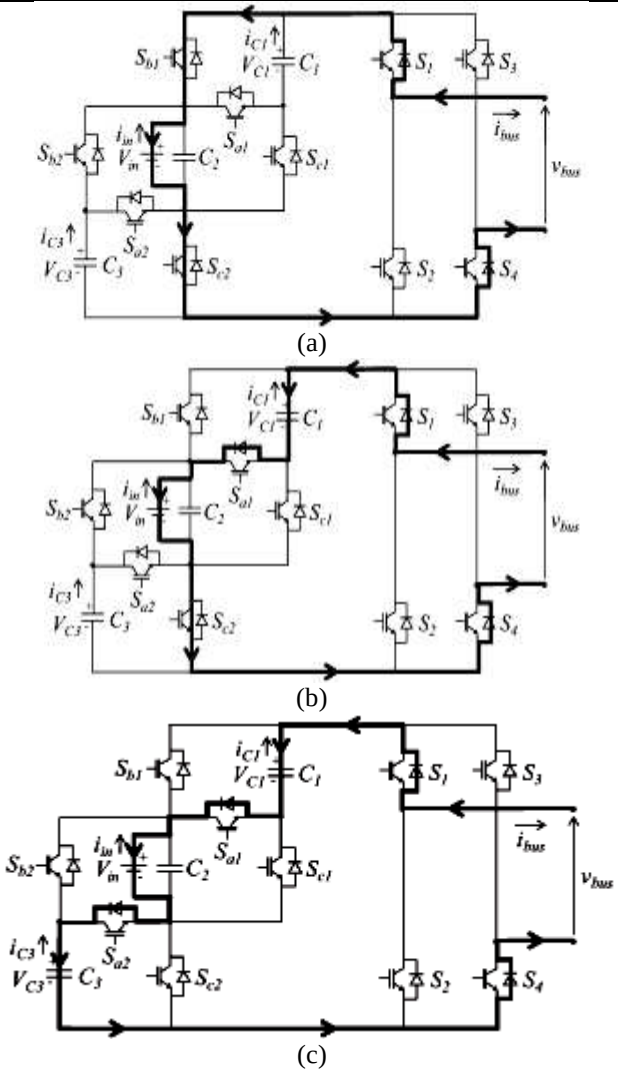

Fig. 4. Current flow of the proposed inverter (n = 2) with an inductive load, (a) all capacitors are connected in parallel, (b) the capacitor $C1$ is connected in series and the capacitor $C3$ is connected in parallel, and (c) all capacitors are connected in series.

When the phase difference φ satisfies $0 < \varphi < \sin{-}1(2/3)$ i.e., $0.745 < \cos\varphi < 1$, the current flows as shown in Fig. 4(a) and (b) before $t = \varphi/2\pi f_{ref}$. Therefore, the capacitor C_1 is charged by the reverse current and the voltage of the capacitor C_1 is increased in the state when C_1 is connected in series as shown in Fig. 4(b). The charge amount Q_1' of the capacitor $C1$ in the state is calculated by

$$Q_1' = -\int_{t_1}^{t_2} D_{Sa1}(t) I_{bus} \sin(2\pi f_{ref} t - \phi)\, dt \quad (10)$$

Where $D_{Sa1}(t)$ is the duty ratio of the switch $Sa1$. From Fig. 3, $D_{Sa1}(t)$ is sinusoidal function between t_1 and t_2. In addition, $D_{Sa1}(t_1) = 0$ and $D_{Sa1}(t_2) = 1$. Therefore, $D_{Sa1}(t)$ is calculated by

$$D_{Sa1}(t) = 3\sin(2\pi f_{ref} t) - 1 \quad (11)$$

From (7) and (10), the maximum discharge amount Q_1 is larger than the charge amount Q_1'. Therefore, the voltage ripple of the capacitor C_1 is determined by Q_1 when $0.745 < \cos\varphi < 1$. When the power factor $\cos\varphi$ satisfies $\cos\varphi \le 0.745$, there is the term when the current direction becomes reverse in all states of the switching devices as shown in Fig. 4. Therefore, the maximum discharge amount Q_1 is calculated by

$$Q_1 = \int_{\frac{\phi}{2\pi f_{ref}}}^{t_3} I_{bus} \sin(2\pi f_{ref} t - \phi)\, dt \quad (12)$$

From (7) and (12), the maximum discharge amount Q_1 is reduced. However, Q_1 is larger than the charge amount Q_1' because the input current is larger than the reverse current with an inductive load. Therefore, voltage ripple of the capacitor C_1 is also determined by Q_1 when the power factor $\cos\varphi \le 0.745$. The maximum discharge amount Q_1 takes the largest value when $\cos\varphi = 1$ because the peak current is accorded to the peak voltage. Hence, when the capacitance C_k is determined for $\cos\varphi = 1$, the proposed inverter can maintain the output waveform for $\cos\varphi < 1$.

5. CONCLUSION

In this paper, a unique boost switched-capacitor electrical converter was planned. The circuit topology was introduced. The modulation methodology, the determination methodology of the capacitance, and therefore the loss calculation of the planned electrical converter were shown. The circuit operation of the planned electrical converter was confirmed by the simulation results and therefore the experimental results with a resistive load and an inductive load. The planned electrical converter outputs a bigger voltage than the input voltage by change the capacitors serial and in parallel. The electrical converter will operate with AN inductive load. The structure of the electrical converter is less complicated than the standard switched-capacitor inverters. Doctorate of the output wave form of the electrical converter is reduced compared to standard the traditional the standard single part full bridge electrical converter because the conventional construction electrical converter.

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