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Design and Implementation of Low Power High Speed VLSI DSP System for Multirate Polyphase Interpolator

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Abstract: **Interpolator is an important sampling device used for Multirate filtering to provide signal processing in wireless communication system. There are many applications in which sampling rate must be changed. Recent advances in mobile computing and communication applications demand low power and high speed VLSI DSP systems. In this paper, an efficient method has been presented to implement low power high speed Multirate Polyphase Interpolator for wireless communication systems. Many architecture developed for the design of low complexity, bit parallel Multiple Constant Multiplications operation which dominates the complexity of DSP systems. However, major drawbacks of present approaches are either too costly or not efficient enough. On the other hand, MCM and digit-serial adder offer alternative low complexity designs, since digit-serial architecture occupy less area and are independent of the data word length. Multiple Constant Multiplications is efficient way to reduce the number of addition and subtraction in polyphase filter implementation. The simulation of parameters is analyzed by using synopsis 45 nm and Xilinx. Experimental results have shown the efficiency of the proposed technique and the analysis of different architecture. This Multirate design methodology is systematic and applicable to many problems.**

Keywords: **VLSI-Very large scale integrated circuit, VHDL-Very high speed hardware description language, DSP-Digital Signal Processing, FIR: Finite impulse response, FPGA: Field Programmable gate array, MCM-Multiple Constant Multiplication**

I.INTRODUCTION:

In many practical application of DSP, there is a problem of changing the sampling rate of a signal, either increasing or decreasing by some amount. Telecommunication system transmits and receives the different types of signals. There is a requirement to process the various signals at the different rates with corresponding bandwidth. A System that employs multiple sampling rates in the processing of digital signals called as "Multirate digital signal processing system". In most applications Multirate systems are used to improve the performance and increased computational efficiency [2]. The two basic operations in a Multirate system are decimation and interpolation. The Multirate techniques are included to reduce the computational complexity. The role of a filter in decimation and interpolation is to suppress aliasing and to remove imaging. Digital Signal Processing has become essential to the design and implementation of high Performance audio, video, multi-media, and communication systems. Interpolator is utilized to increase the sampling rate as shown in following Figure.

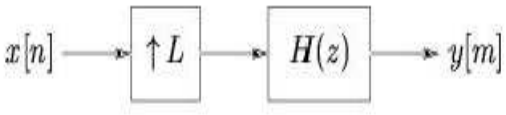

Fig.1.Block diagram representation of Interpolator

The efficiency of FIR filters for sampling rate conversion is significantly improved using the Polyphase realization. Filtering is embedded in the interpolation process and a polyphase structure is used to simultaneously achieve the interpolation by a given factor but running at a low data rate [6].

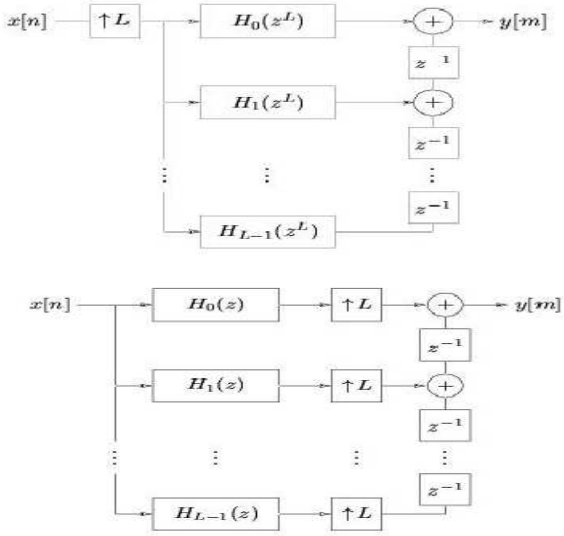

Fig.2 (a-b) Block diagram representation of Polyphase Interpolator

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The FIR filter performs the weighted summation of input sequence and is widely used in mobile communication systems for channelization, channel equalization, pulse shaping and matched filtering due to their properties of linear phase and absolute stability [9]. In Interpolation Multirate filters, the normalized transition bandwidth inversely relates to the interpolation factor *L*. The order of an interpolation filter increases as L. Polyphase is a way of doing sampling rate conversion that leads to very efficient implementations. Sampling rate reduction is required for efficient transmission, and a sampling rate increase is required for the regeneration of the speech. It can be efficiently implemented using finite impulse response digital filters [11].It is found that efficient implementations of low pass FIR filters could be obtained by a process of first reducing the sampling rate, filtering, and then increasing the sampling rate back to the original frequency. FIR based filtering is advantageous in many digital signal processing systems due to the possibility of exact linear phase and freedom of stability problems. Recently, several schemes have been proposed to reduce the arithmetic complexity of FIR structures, e.g., sub expression sharing, multiple-constant multiplication and multiplier blocks [1][4].

II. DESIGN METHODOLOGY:

The digital filters employed in mobile systems must be higher order and realized to consume less power at high speed. Low power, High performance is two most important criteria for many signal processing system designs. Particularly, real time multimedia applications; there have been many approaches to achieve this goal at different implementation level. We have introduced a new architecture based low power and high performance design technique. i.e. Multirate approach and combine it along with DSP techniques such as shifting, carry look ahead and folding to design several DSP blocks like FIR and Polyphase filtering. In this paper, we design Multirate Polyphase Interpolator in direct form, transposed form, using MCM and Digit serial adder. As shown in Fig. 1, the hardware block called a multiplier block is used to implement all coefficient multiplications. The concept of the multiplier block is significant in both terms of
area and power because some adders and shifters can be shared among different multiplications [6].

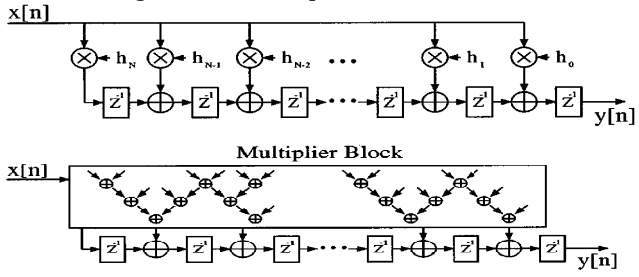

Fig. 3(a-b) FIR Filter structure (a) General transposed form
(b) Multiplications are replaced by a multiplier block

The digit-serial MCM operation in shift-add architecture consists of digit-serial addition and subtraction operations, and D flip-flops for the shift operations, as opposed to the bit-parallel MCM operation, where shifts are free in terms of hardware. The complexity of the resulting realization will be depending on three factors. First, the size, numbers, and type of MCM blocks. Second, the number of delay elements, and, finally the number of structural additions, i.e., the additions that are not part of the MCM block [10]. Another concept can be used to optimize the parameters is multiplication using shifts, additions, and subtractions realization without general multipliers. The number of additions and subtractions can be significantly reduced by using common partial results. As additions and subtractions have similar complexity as an example [7], consider the constant multiplications 29*x* and 43*x*. Observe from Figure 4 that the sharing of partial products 3x and 5x reduces the number of operations from 6 to 4. The decompositions of 29*x* and 43*x* in binary are listed as follows:

$29x = (11101)_{bin}\ x = x<<4+x<<3+x<<2+x$ ------ (I)
$43x = (101011)_{bin}\ x = x<<5+x<<3+x<<1+x$ ----- (II)

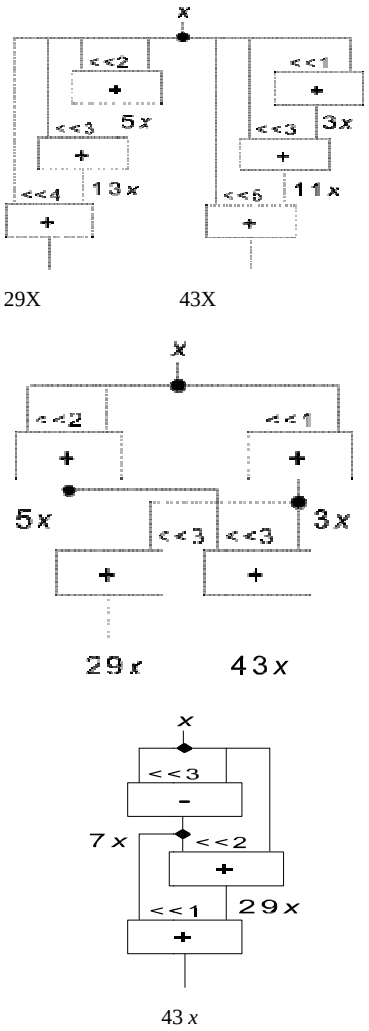

Fig. 4. Shift add implementation of 29*x* and 43*x* (a) without partial product sharing (b) with partial product sharing

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The problem of designing Polyphase interpolator has received a great attention due to large number of multiplications. This implementation must satisfy the enforced sampling rate constraints of the real time DSP applications and must require less space and power consumption. Present works have focused on design of Multirate Polyphase interpolator by filters, data generator latches and adder. As the coefficients of an application specific filter are constant, the decomposition is more efficient than employing multipliers [6]. The complexity of FIR filters in this case is dominated by the number of additions and multiplications [10]. The multiplier block of the digital FIR filter in its direct form is implemented in the design so that significant impact on the complexity and performance of the design will be improved. Also, Polyphase interpolator is designed using MCM and digit serial adders which overcome problem of complexity, design performance and producing very low area [20]. Authors have used the above mentioned techniques to reduce the complexity in the design. In this, Polyphase interpolator filter with a factor of 18 is designed using three cascaded filters. The impulse response is obtained by convolution of three vectors with 18 ones in each, The trade-off between additions and delay elements is circuit and technology dependent, and, hence, should be evaluated on the circuit level. Digit serial systems have become attractive for digital designers in the recent years. These systems process multiple bits of the input word, referred to as the digit size, in one clock cycle. For a digit size of unity, the system reduces to a bit serial, and for a digit size equal to the word length, the system reduces to a bit parallel system. It process one whole word of the input sample in one clock cycle, are ideal for high speed applications [16].

III.RESULT:

I] Following figure 5(a) – (d) shows direct form of Polyphase Interpolator which uses latches in direct form, this system is very efficient because it required very less power dissipation and maintaining higher speed. But, this design consumed more area.

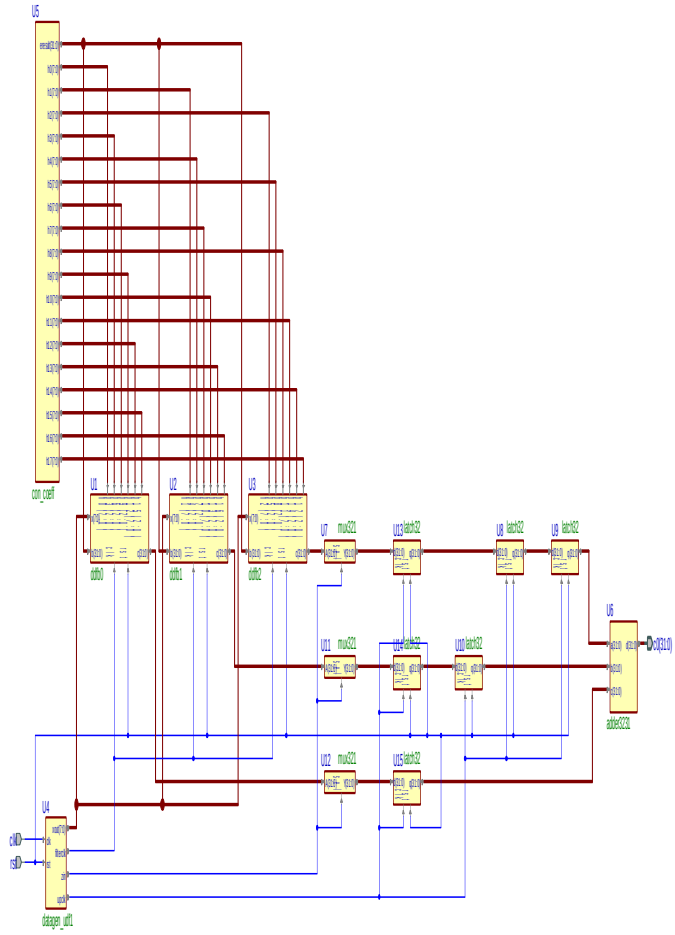

Fig. 5(a) RTL view of Polyphase Interpolator in direct form

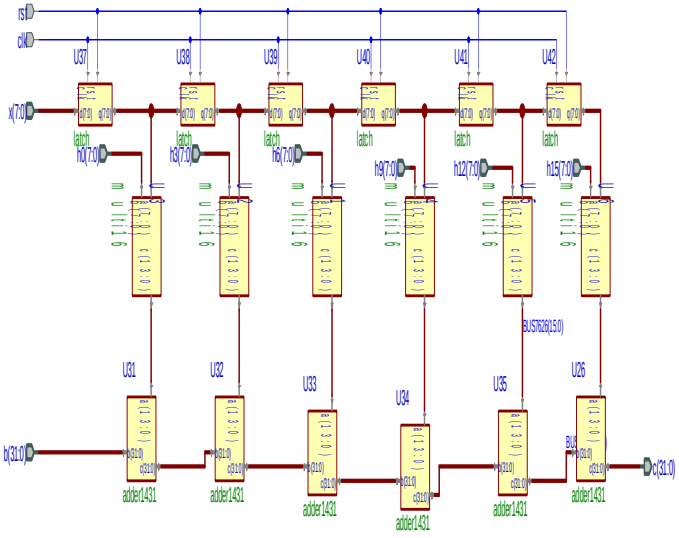

Fig. 5(b) Internal structure of polyphase filter

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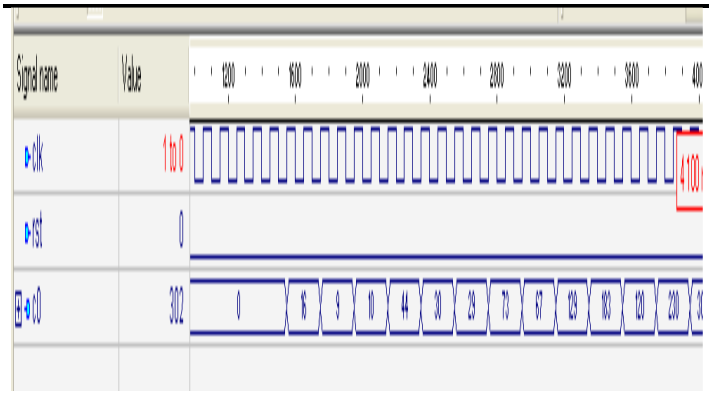

Fig.5(c) Design waveform

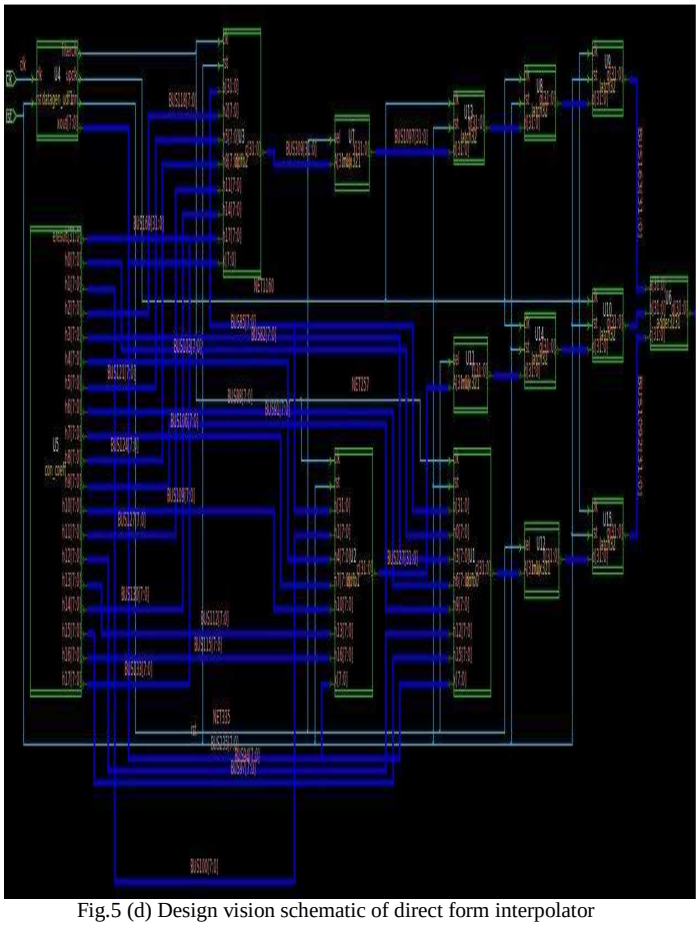

Fig.5 (d) Design vision schematic of direct form interpolator

II] Following figure 6(a)-(d) shows transpose form of Polyphase Interpolator. This design uses latches in transpose form. Therefore, this system also required more area maintaining moderate power dissipation and speed.

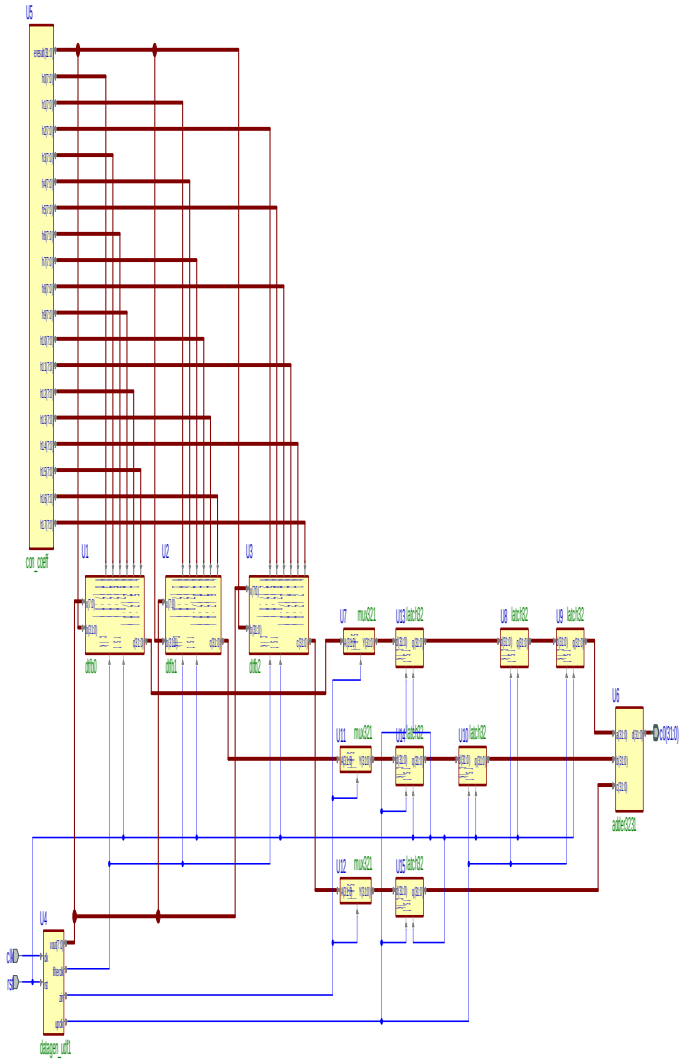

Fig. 6(a).Multirate Polyphase Interpolator in Transpose form

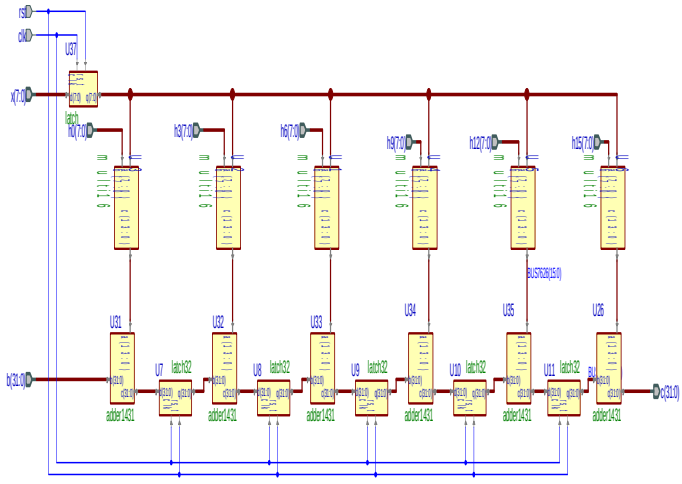

Fig. 6(b) Internal structure of polyphase filter

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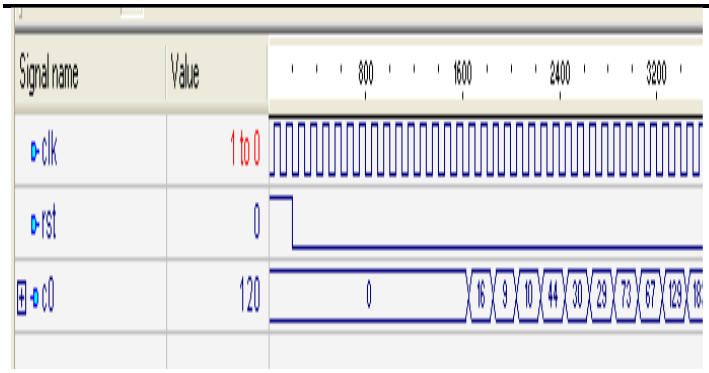

Fig.6(c) Design waveform

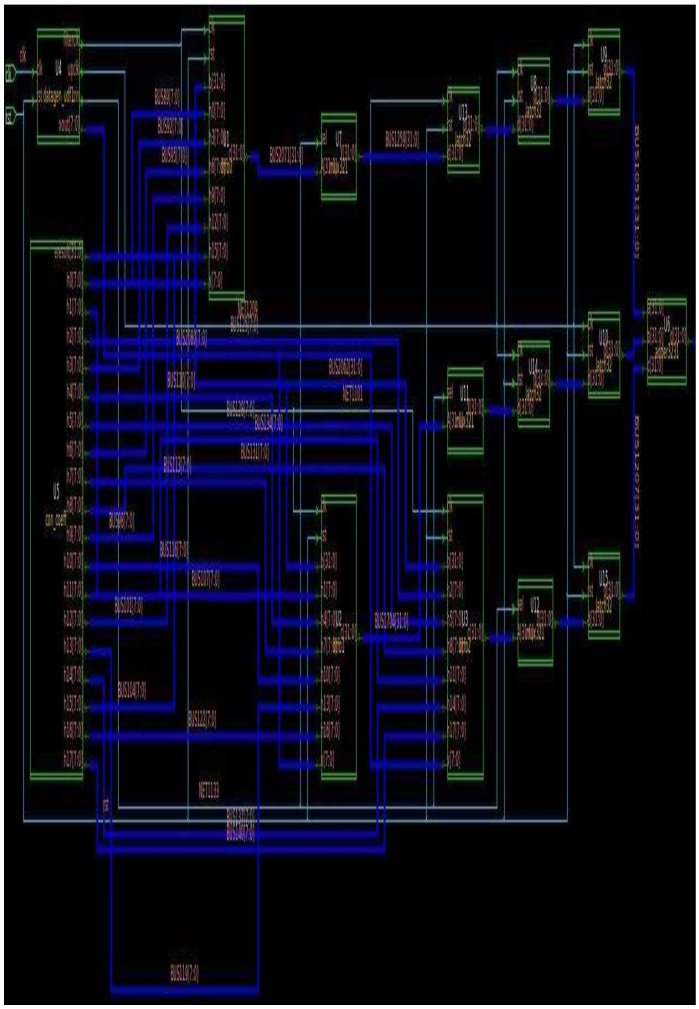

Fig.6(d) Design vision schematic of Polyphase Interpolator in Transpose form

III] Authors efforts are directed towards reduction of area at great extend succeeded by using MCM of Multirate Polyphase Interpolator. This design consumed moderate power.

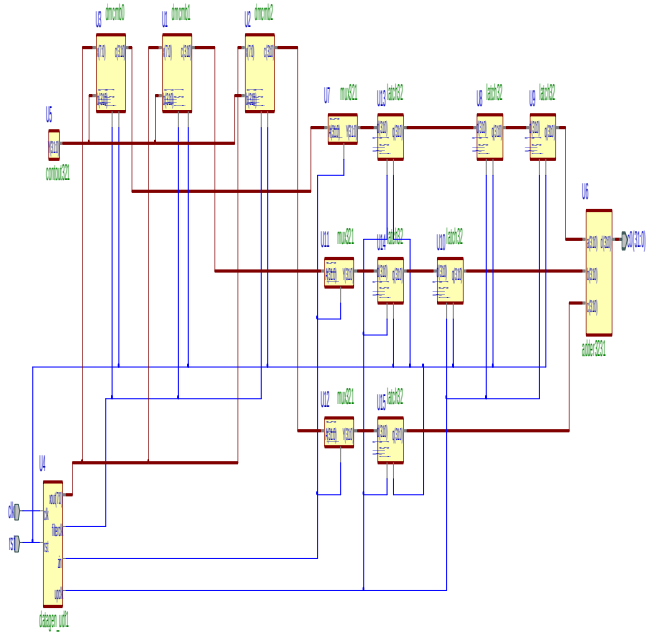

Fig. 7(a).Multirate Polyphase Interpolator using multiple constant multiplications

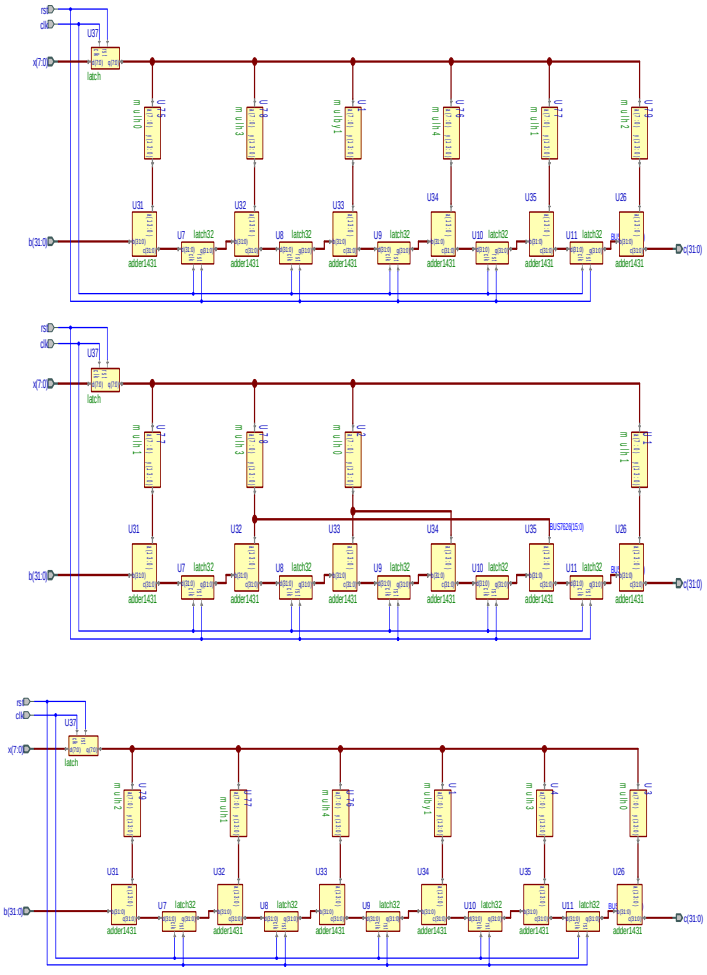

Fig. 7(b) Internal structure of polyphase filter

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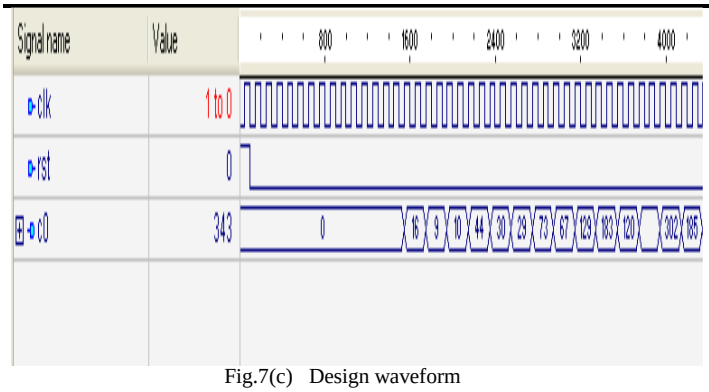


Fig.7(c) Design waveform

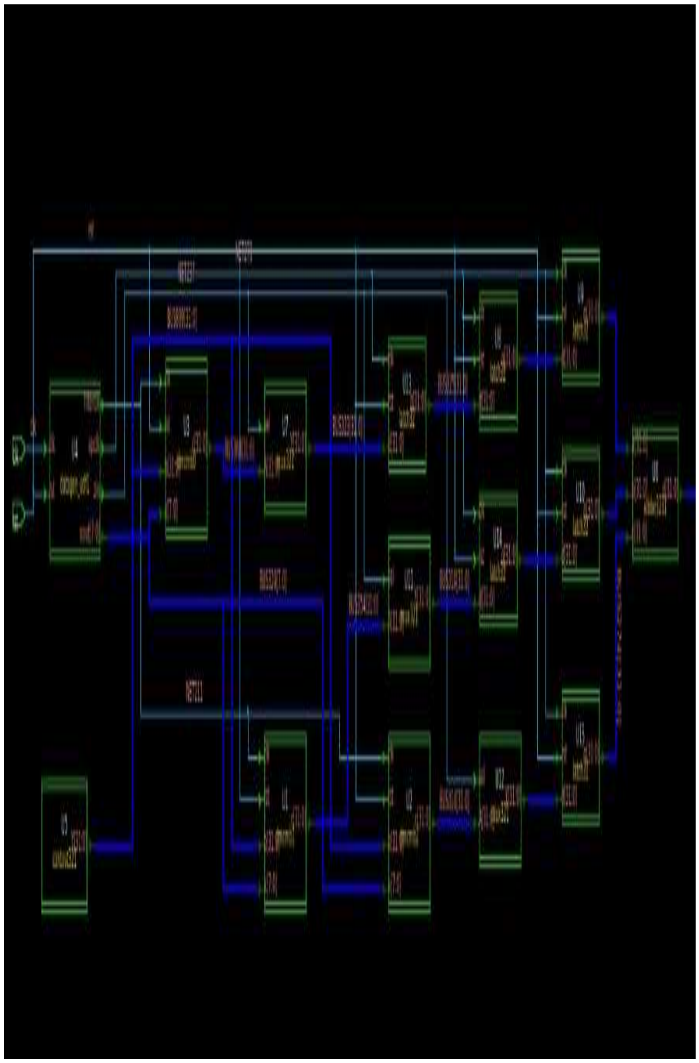


Fig.7(d) Design vision schematic of polyphase Interpolator using multiple constant multiplication

IV] Following figure 8(a)-(d) shows transpose form of Polyphase Interpolator which uses MCM & digit serial adder. This system required less area and maintaining higher speed.

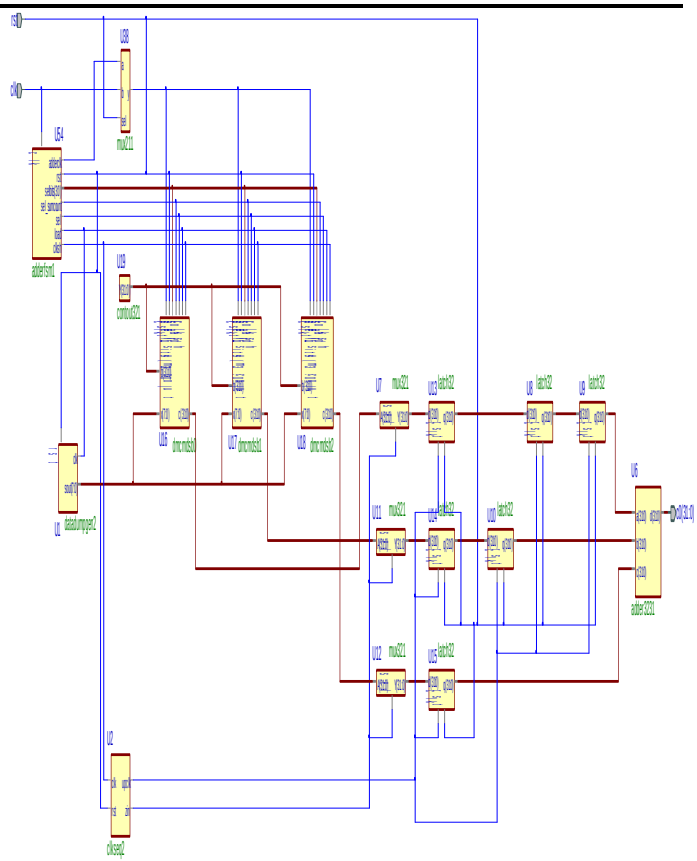
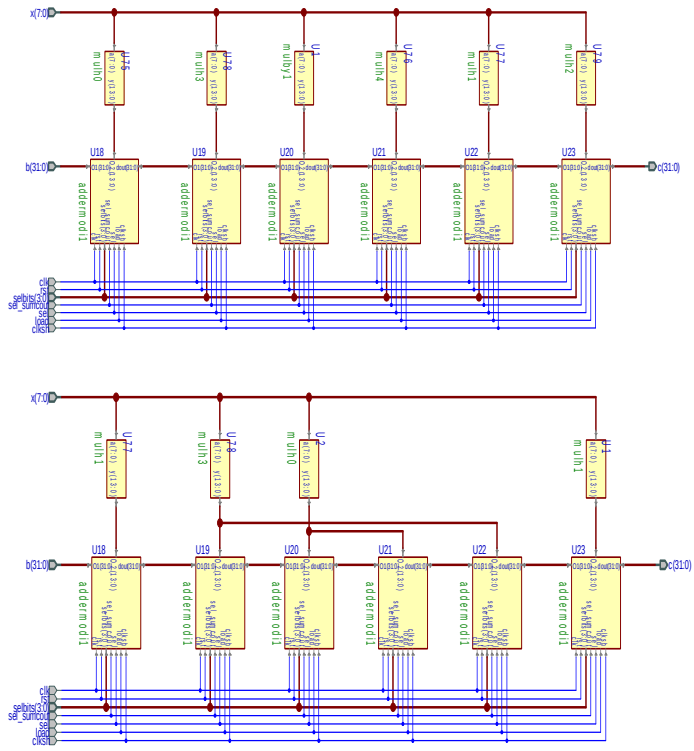


Fig. 8(a) Multirate Polyphase Interpolator using MCM & Digit serial adder



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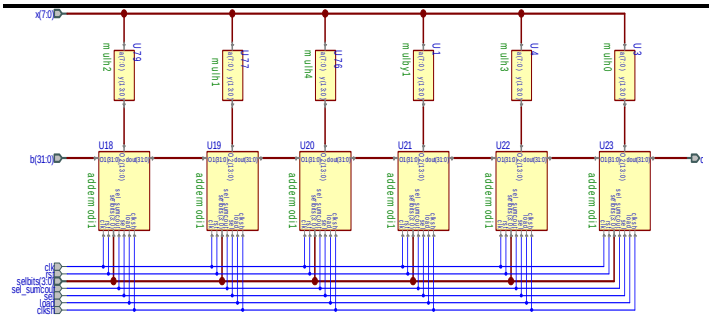

Fig.8 (b) Internal structure of Polyphase Filter

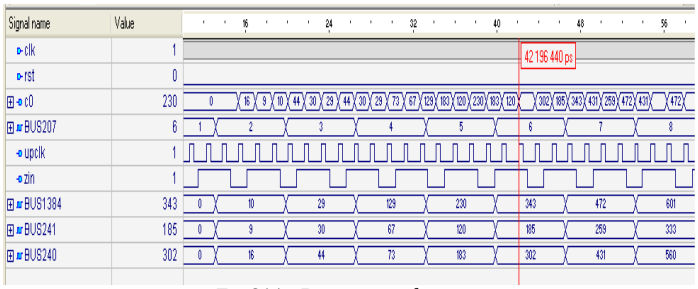

Fig.8(c) Design waveform

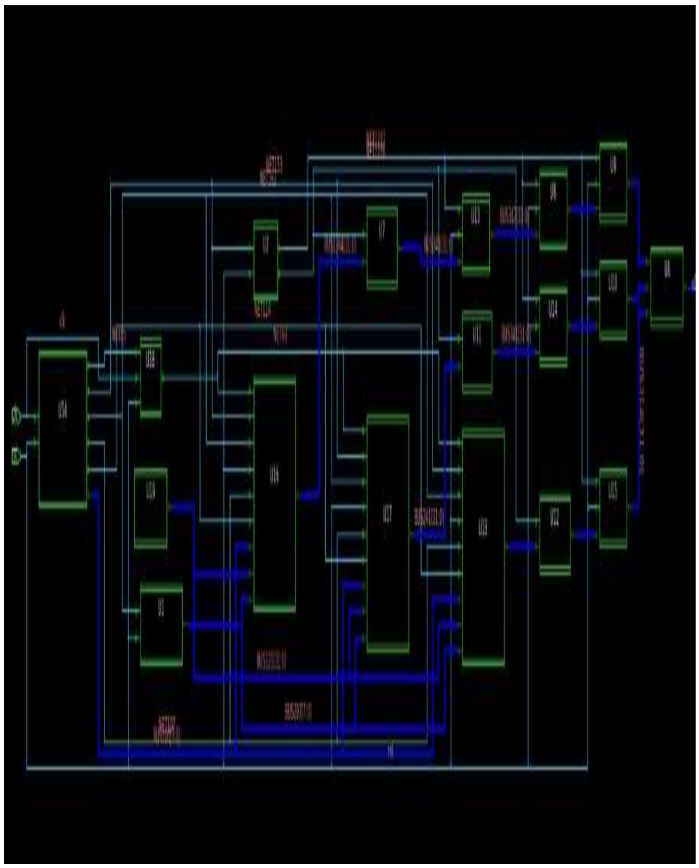

Fig.8(d) Design vision schematic of Polyphase Interpolator using MCM and digit serial adder

The Multirate Polyphase Interpolator is implemented on FPGA cyclone –II device which shown complete setup of the design as follows:

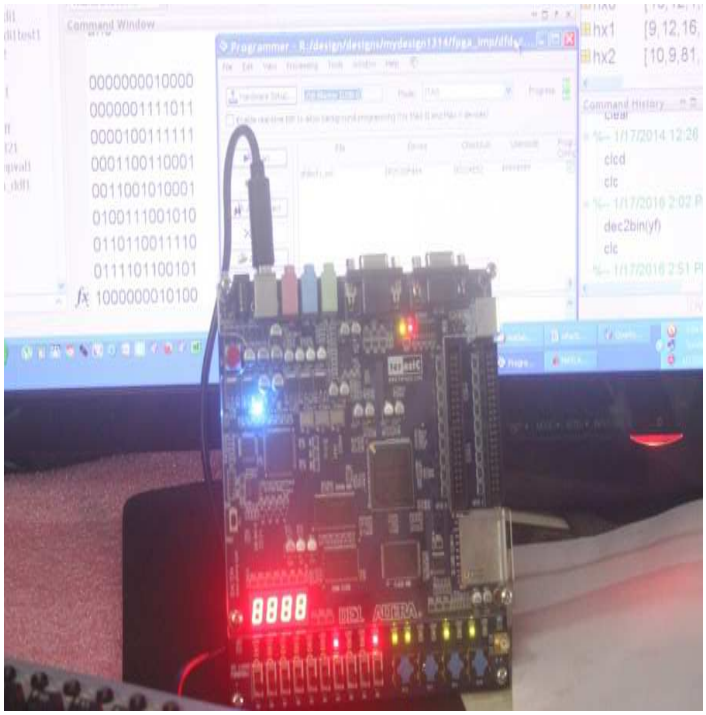

Fig. 9 Complete set up of design of Multirate Polyphase Interpolator showing output 10011100101

TABLE 1

Type	*Area[um^2]*	*Power (uw)*	*Speed (MHz)*
Direct Form	**31921**	**113**	**205.634**
Transpose Form	**37511**	**222**	**106.315**
Using MCM	**14747**	**220**	**103.189**
Using MCM and Digit Serial Adder	**23178**	**413**	**151.579**

Following graphs shown comparative analysis of parameters of Multirate Polyphase Interpolator using different techniques

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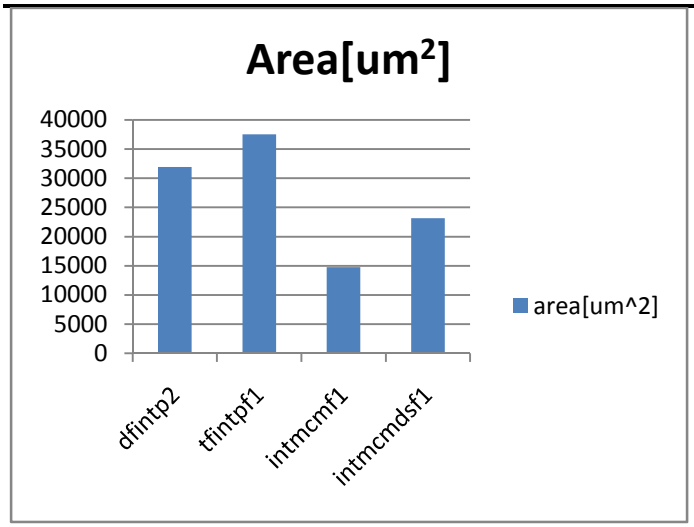
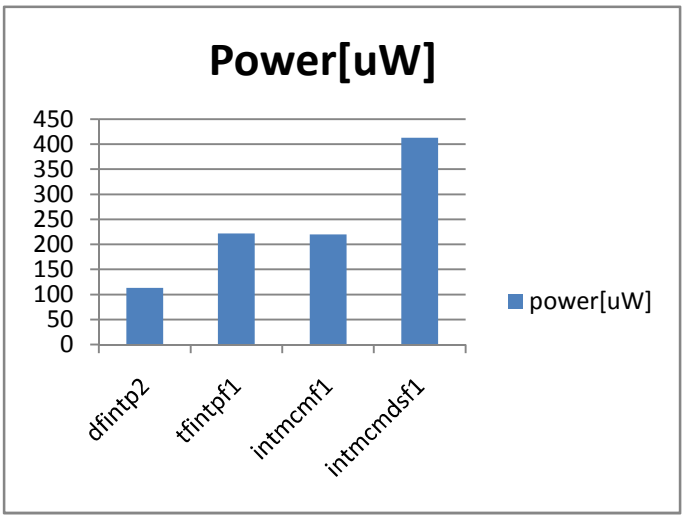
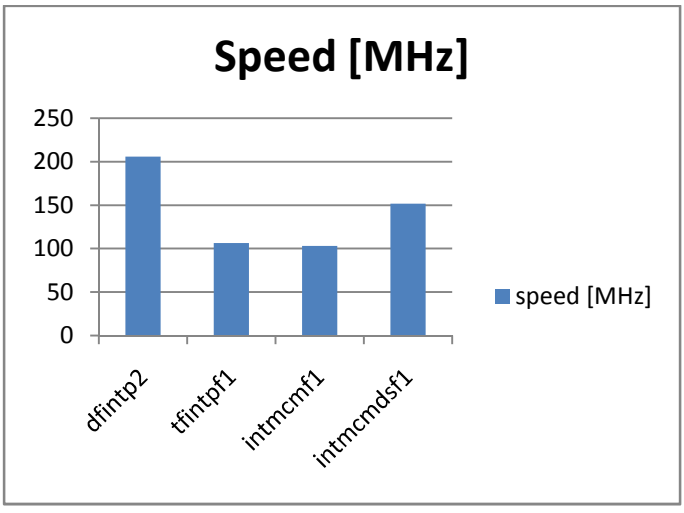


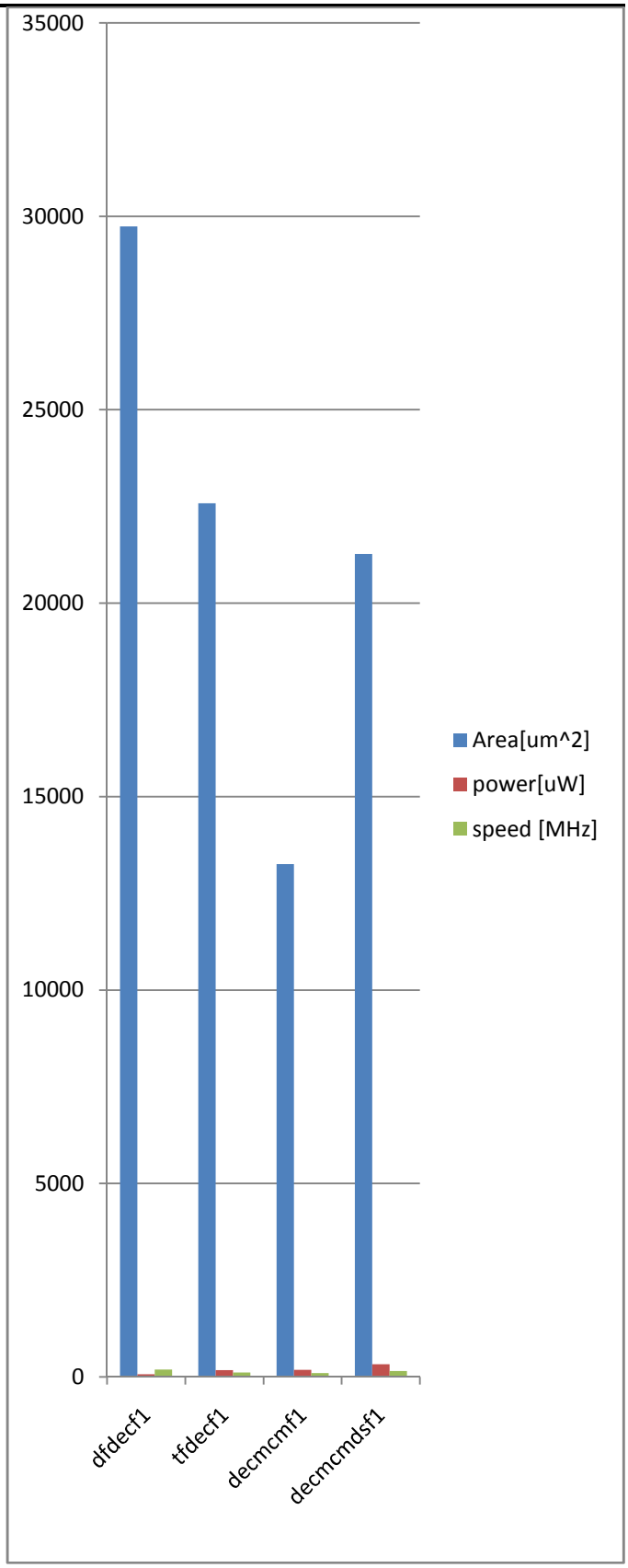
Graph 1



Graph 2



Graph 3



Graph 4

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IV.CONCLUSION:

Authors have presented the different optimization techniques and methodology for Multirate Polyphase Interpolator. We have used Active-HDL and Quartus-II for the simulation and done the synthesis of the design on FPGA platform. The parameters are analyzed by using synopsis 45 nm and Xilinx software. Multirate Polyphase Interpolator is designed in its direct form, Transpose form, using MCM and using Digit serial adder which provides power, area and speed for system. The results are given separately and comparison in tabulation form found satisfactory. Physical testing verified that implementation worked correctly. MCM and digit serial adder technique reduces the area of the system to a great extent and overcome problem of complexity, design performance. Direct form of Multirate Polyphase Interpolator is best suited for implementation of DSP system which requires very less power dissipation maintaining higher speed. The proposed methodology provides a systematic way to derive low power, high speed system.

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