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# 32-bit High Speed Adder

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***Abstract*— Fast mathematical operations are need of today's processors. Fast mathematical operation depends upon adder circuits. Different approaches used to implement fast adders. Carry Select Adder (CSLA) is used for fast addition. Carry Look Ahead Adder (CLA) is also one of the fast adder but it has limitation. If CSLA is implemented by level 2 logic CLA will be the fast adder. Level 2 logic CLA used carry look ahead block to generate output carry by skipping addition blocks. It will also reduces area as compare to CSLA. Level 2 logic CLA can also be used to implement n bit adders.**

***Index Terms*— C***arry look ahead adder, carry* ***select adder, level2 logic CLA, delay.***

## I. Introduction

Carry propagation delay is important factor for designing adders. The 32-bit adders are implemented using 16-bit adders, 16-bit adders are implemented using 8-bit adders, 8-bit adders are implemented using 4-bit adders. There are four types of adder. Ripple carry adder, Carry look ahead adder, carry select adder and carry skip adder. Each adder has different techniques to generate output carry therefore each adder has different carry propagation delay. The lower bits adder output carry is the input carry of upper bits adder. Therefore the lower bits adder should reduce the carry propagation delay.

## II. Delay Estimation in Basic Adder Units

Every digital gate (AND, OR, NOT, EXOR...) has its own propagation delay depending upon technology being used [3]. As shown in Fig.1, two inputs A and B applied at same time to AND gate but the output is delayed by Tp. This is called gate propagation delay.As shown in fig.2 the total delay for the output SUM is the sum of delay of EXOR1 and EXOR2 gate. Let us assume propagation delay of each gate is 2ns, then total delay of output sum is 4ns .In the same way, output carry will have total delay of 6ns as it passes through EXOR1, AND2 and OR1.This is longest path for output carry. Output carry also depends upon AND1, but propagation delay of AND1 gate and EXOR1 is same because they are working parallely. OR1 gate accepts two inputs, one is 4ns delayed signal and another is 2ns delayed signal. Therefore, the correct result of output carry can be obtained after 6ns only. As shown in fig.3, the full adder requires 2GD.

The carry propagation delay is the delay required by adder circuit to generate output carry through the longest path. The carry propagation delay of full adder is 2 GD. In this paper all delays for carry and sum are tabulated by considering each gate delay as 2ns.

## III. Carry Propagation Delay of Four Bit Adders

### A. Ripple Carry Adder

The RCA is the slowest adder because the carry of previous stage is connected to next stage as shown in fig.4.

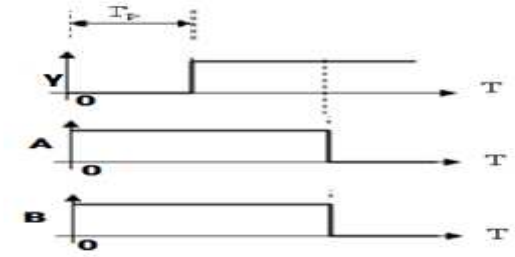


Fig.1 Propagation delay of two input gate.

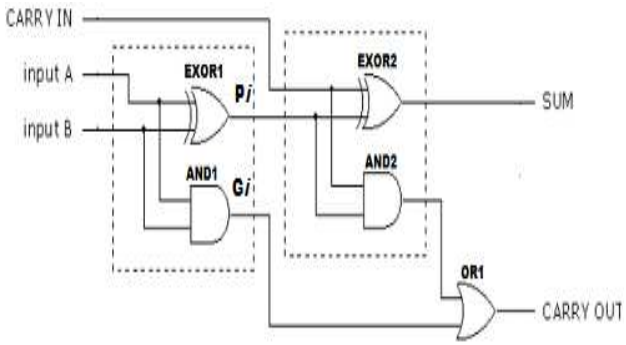


Fig.2 Full Adder using two half adders

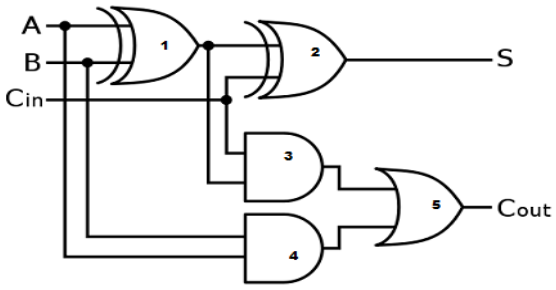


Fig.3. Full adder

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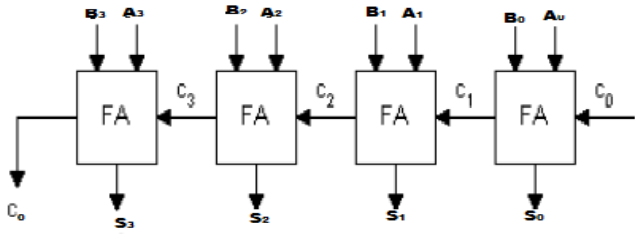


**Fig. 4 Four bit Ripple Carry Adder**

Hence the carry propagated like ripple from LSB stage to MSB [3].

B. Carry Look Ahead Adder

In this the carry signal is calculated in advance based on input signals as it is operated on two internal signals called carry generate(G*i*) and carry propagate(P*i*).These signals are defined as

$$Pi = Ai \text{ (EXOR) } Bi \quad (2)$$

$$Gi = Ai \text{ (AND) } Bi \quad (3)$$

The input carry propagate to the output carry whenever P*i* = 1 and Co is generated whenever Gi = 1 regardless of input carry Ci. These signals settled to their steady state value after propagation to their respective gates. The output sum (Si) and output carry (Co) can be defined as

$$Si = Pi \text{ (EXOR) } Ci \quad (4)$$

$$Co = Gi \text{ OR ( } Pi \text{ AND } Ci) \quad (5)$$

The SOP equations for output carry at various stages is as follow referring equation 2 to 5.

$$C_1 = G_0 + P_0C_0 \quad (6)$$

$$C_2 = G_1 + P_1C_1$$
$$= G_1 + P_1 (G_0 + P_0C_0)$$
$$= G_1 + P_1G_0 + P_1P_0C_0 \quad (7)$$

$$C_3 = G_2 + P_2C_2$$
$$= G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0 \quad (8)$$

$$C_4 = G_3 + P_3C_3$$
$$= G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0 \quad (9)$$

The main disadvantage of CLA adder is that gate complexity increases as number of bit for addition increases [4]. 2-bit and 4-bit carry look ahead adder implementation is easy. But 8-bit,16-bit carry look ahead adder implementation is difficult because as number of bit increases number of AND gate increases and number of inputs of AND gate and OR gate also increases. Fan in (number of input pins of gate)of AND gate and OR gate is restricted . Other fast adders like CSLA, CSKA can be used. Output sum propagation delay for So is 2 GD and for S1, S2, S3 is 4GD. Output carry propagation delay is 3GD as shown in fig.5. As carry is generated earlier than S1, S2, S3, it is called as CLA level block accepts group generate and group propagate signals and process them to generate output carry.

C. Carry Select Adder

In CSLA, inputs bits are divided equally into two parts, upper bits and lower bits [1]. Three adders are used in this case; one for lower bits addition and two for upper bits addition. One upper bit adder perform addition with assumption that input carry($C_{in}$) = 0 and other perform addition for $C_{in}$ =1 . Output carry bit of lower bit adder ($C_{ol}$) select either of two upper adders as shown in fig.4 as it is connected to select pin of each MUX as shown in fig.7.

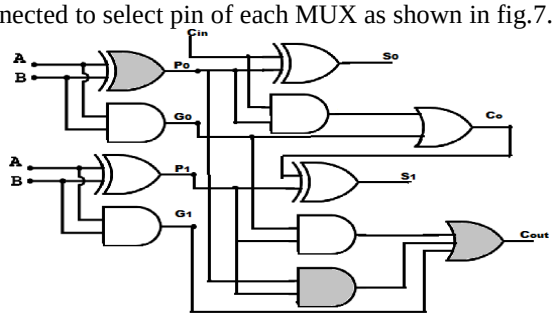


Fig. 5 Two -bit CLA.

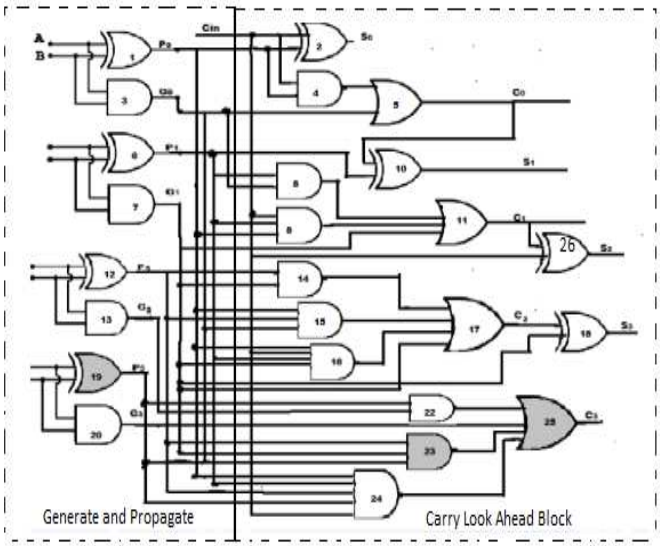


Fig. 4 Four bit CLA.

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As upper bit adders and lower bit adder perform addition simultaneously, the speed of addition increases. But as number of adder unit increases and additional multiplexers are required, the area requirement increases. If n bit CSLA (n/2+1) MUX are required.

In this two full adders as shown in fig.2 are cascaded in such a way that output carry of first 1-bit adders is input carry of next 1-bit adder.

D. Previous work:

16-bit CSLA hierarchy is shown in the Fig……

Here16-bit adder when implemented using three 8-bit CSLA of three 4-bit CLA is the fastest adder. The carry propagation delay is mentioned with GD. 4-bit CSLA requires only 3GD for output carry. Three four bit CLS used to form 8-bit CSLA. The carry output of lower 4-bit CLA is given to MUX select input. Three 4-bit CLA will generate output carry simultaneously. MUX circuit requires only two gate delay. Therefore 8-bit CSLA using three 4-bit CLA will have total carry propagation delay as 5 GD. Now this three 8-bit CSLA used to implement 16-bit CSLA then total output carry propagation delay is 7GD.

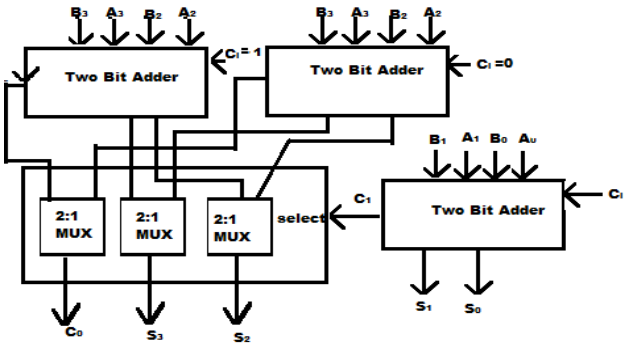


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**Fig.7 Four bit carry select adder**

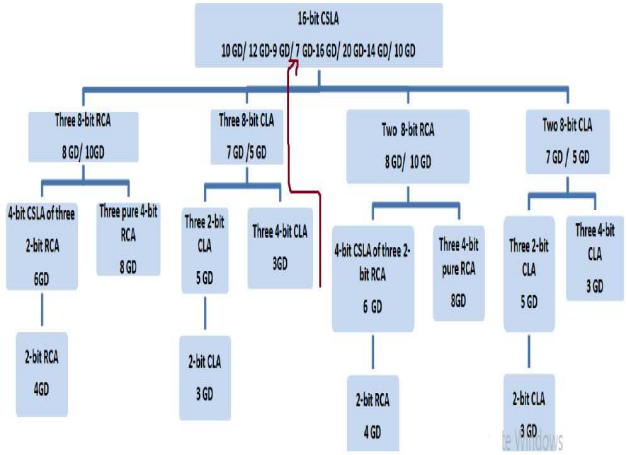


Fig 8. 16-bit adder hierarchy

E. Level 2 CLA

To reduce carry propagation delay new carry look ahead is used. CLA adder basically divided into two parts. One part generates only propagate and generate signal and another part will generate output carry. The clock which accepts generate, propagate signals and produces output carry is called Carry Look ahead block. This carry look ahead block can is used at top level of 16-bit, 32-bit adders. The lower level will only generate propagate and generate signals. This lower level is also responsible for output sum. The 5-bit CLA is shown in fig…

The 5-bit CLA requires only 2-bit carry look ahead block and two CLA. One is 2-bit CLA and another 2-bit CLA. The group propagate and group generate signals are given to top level.

$$P_{0\text{-}1} = P_0 \,.\, P_1 \; ; \qquad (10)$$

$$P_{2\text{-}4} = P_2 \,.\, P_3 . P_4 . \qquad (11)$$

$$G_{0\text{-}1} = G_1 + G_0P_0 \qquad (12)$$

$$G_{2\text{-}4} = G_4 + G_3P_3P_4 + G_2P_2P_3P_4 \qquad (13)$$

Output carry is generated only when MSB generate the carry or if LSB generates the carry then MES bit should propagate the carry. For 3-bit CLA ,if G4 generates the carry then it will be the output carry of 3-bit CLA. If G3 generates the carry then P3 and P4 signals should propagate the carry. If G2 generates carry then P2, P3, P4 should propagate the carry.

This logic is used to implement 16-bit CLA. For this four 4-bit CLA are used along with 4-bit carry look ahead block. Group generate and group propagate signals are generated at lower level module.

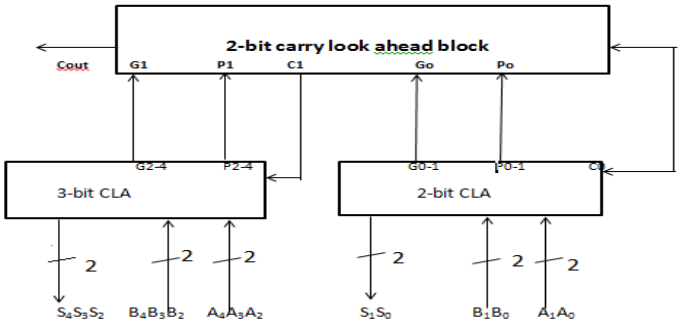


**Fig.7 Five bit CLA**

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Result and conclusion

The carry look ahead adder has minimum carry propagation delay. If it is implemented by using propagate and generate signal then fast adder is implemented. It requires only 7 GD.

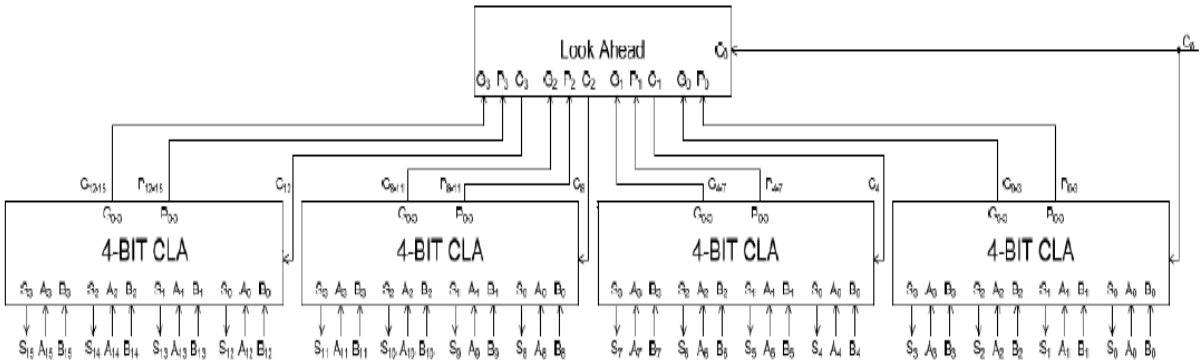


Fig 8. 16-bit CLA

TABLE V

DELAY ANALYSIS OF 32-BIT CSLA ADDERS

| S.No. | Parameters | 32-bit CSLA Using three 16-bit adders | |
|---|---|---|---|
| | | Hierarchical CLA | CLSA |
| 1 | Level of logic | 19 | 14 |
| 2 | No. Of slice | 68/768 | 73/763 |
| 3 | Memory usage | 252196 | 258916 |
| 4 | Logic delay(ns) | 14.001 | 11.02 |
| 5 | Route delay(ns) | 14.220 | 10.782 |
| 6 | Total delay(ns) | 28.231 | 21.824 |

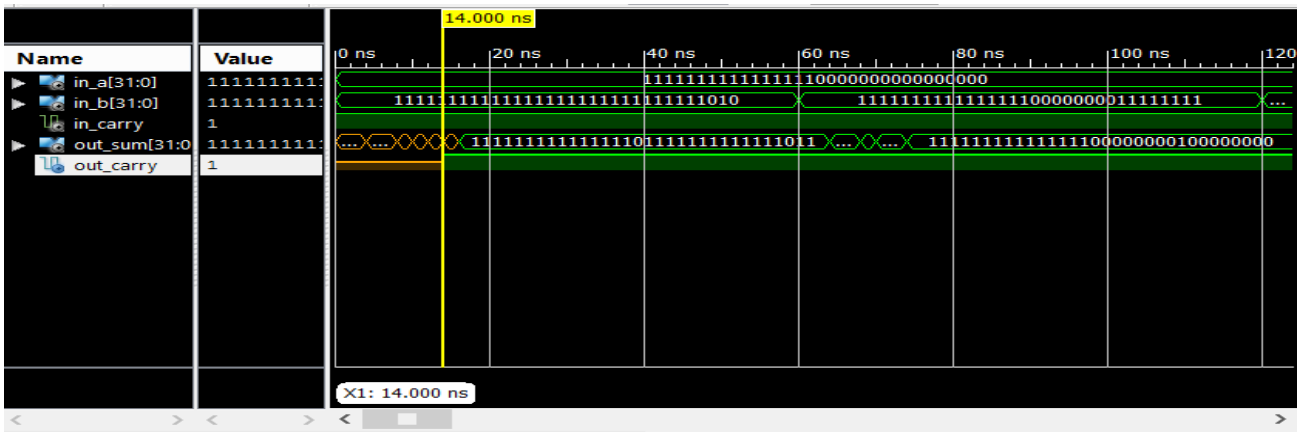


Fig. 9 Test bench waveform of 32-bit high speed adder

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