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Microprocessor Hardware Self-Test Architecture for On-Line Testing

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***Abstract*— The technique proposed forces the processor to execute a compact SBST-like test sequence by using a hardware module called Microprocessor Hardware Self-Test (MIHST) unit, which is intended to be connected to the system bus like a normal memory core, requesting no modification of the processor core internal structure. MIHST method guarantees the same or higher defect coverage than the traditional SBST approach, it reduces the time for test execution.**

***Keywords*—Microsoft Hardware software based self-test (sbst), built-in self-test(bist),functional test, verification**

I. INTRODUCTION

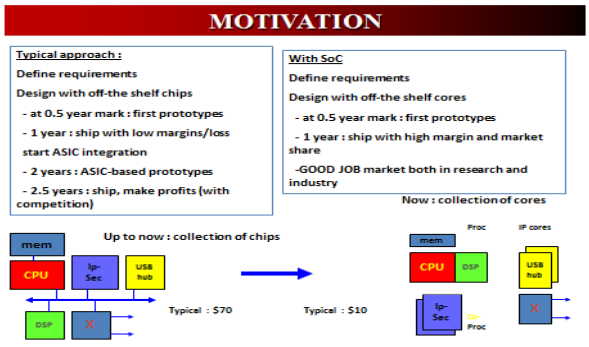


Fig.1

The Fig.1shows the motivation for choosing the field of verification. As the technology updates, it is making the design complicated, the verification is done rigorously to obtain the 100% fault free designs.

II. COMPARISON

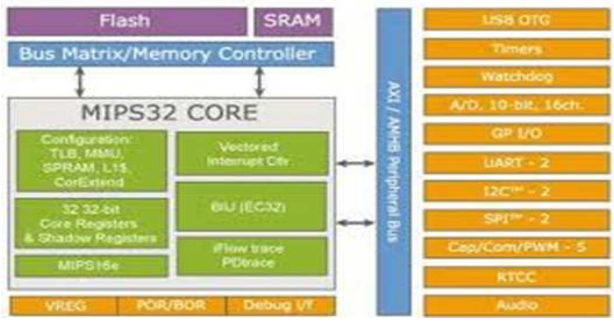
Comparison of MIHST with original SBST

MIHST	SBST
➢ IT DOES NOT DEPEND ON THE PROCESSOR REQUEST,THEY EXECUTE PREDEFINED INSTRUCTIONS,ADDRESS IS NOT CHANGED.	➢ THEY ARE PROCESSOR DEPENDENT FOR THE EXCECUTION,THEY RISE THE EXCEPTIONS DUE TO THIS THE ADDRESS OF THE INSTRUCTIONS MAY GET ALTERED
➢ THEY REDUCE THE RESOURCES REQUIREDFOR THE TEST	➢ WITH PURE SBST THIS IS NOT THE CASE
➢ THE SYSTEM MEMORY IS NOT REQUIRED TO STORE TESTCODE	➢ PURELY SYSTEM DEPENDENT
➢ THEY HAVE GOOD CONTROL AND THE EXECUTION FLOW OR LOGIC FLOW,REDUCES THE EXECUTION TIME	➢ REQUIRE LENGHTY CODE ,REQUIRE SEPARATE CODE STURUCTURE TO AND INCREASE THE EXECUTION TIME
➢ Provide good IP protection.	➢ Integrity of IP are less protective.
➢ Good security because code will be in encoded form saves the processor from attacker before they update MIHST form.	➢ Code structure is in direct form and lengthy.
➢ Costwise very effective because of reusability.	➢ Cost depends on the complexity of the system under test.
➢ Drawback initially they require more development time due to customization	➢ Less compared to MIIIST.SBST Imposes zero hardware and efficiently used in periodic online testing but lacks the programmable MBIST

II. PROPOSED APPROACH

Based on the type of BIST called MIHST, MIHST is in the form of IP and connected to the bus and usually intervenes during the test mode. MIHST behaves mainly on the two principles. The system may be either in the normal or in the test state; in the former, the processor executes the instructions read from the code memory; in the latter, the MIHST unit generates and provides an instruction stream to the processor core, while also observing the processor behaviour. When generating the instruction stream, the MIHST unit does not care about the sequence of instruction addresses generated by the processor for instruction fetch purposes. The MIHST unit internally encodes the test program in a custom manner that exploits the test program regularity, minimizing the hardware required to store it. To test the above approach, let us consider MIPS as the processor for the implementation purpose.

IV. REASONING FOR CHOOSING THE MIPS



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1. Its is32-bit processor.
2. it supports 4-stages of pipeline:
   - ID(Instruction Decode
   - IF(Instruction Fetch)
   - EX(Instruction Execute)
   - ST(Store Result)
3. CPU register memory, each location stores 32-bit of data.
4. Data memory--> incorporated it with register file and provided option to port the data through output port.
5. Instruction Memory(ROM) stores instructions, each 32-bit wide.
6. Input or output PORTS are available so that user can provide Input data and also monitor/access any register data through Output Port.--> this very important feature.
7. Supports ALL instructions given in the paper.
8. optimised Control unit such that it generates only useful control signals.

Area/power improvement
1.No unnecessary control signals generation.
2.Cheaper in cost.
Hence User-friendly
Provided Input and Output Ports:
User can store any data into register file through Input port which provides flexibility
User can access any register data, monitor it and try to verify, if its correct or not through Output Port

Applications:
Mobile Multimedia
Handheld Multimedia
Home Electronics
Mobile Computing
Design Visualization
Media & Entertainment
Automotive
Networking
Applications OF EMERGING Markets

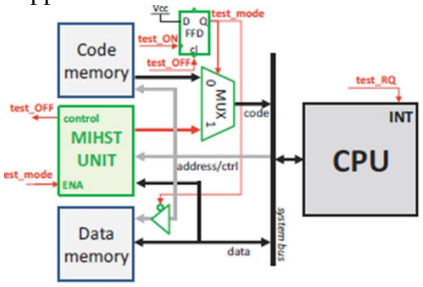

Fig.3 Proposed Architecture

Overcomes some limitations of pure SBST
A MIHST test always finishes Address generation is no longer a problem because the processor receives instructions autonomously provided by the MIHST.
1. It makes the program code structure simpler, since there is no need to respect semantic constraints.
2. Branches and all address related functionalities are tested by simply spying the bus, without the need for storing a test program distributed over the whole memory space.
3. Since the execution flow is not controlled by the processor, to obtain correct data memory accesses and it is a effective methods to test complex features such as forwarding paths and stalls of the pipeline.

The architecture of the MIHST unit includes:
An instruction register, holding the value to be put on the bus when the CPU performs a read cycle.
A set of internal memories for storing the encoded information about the instructions to be generated, resorting to an ad-hoc instruction set including:
1> OPCode words, identifying instructions and including information about their execution under the MIHST unit control
2> OPErand words, describing operands to be applied and their evolution along the program.
The internal memories can be implemented in RAM and the encoded test program , in this case will be hardwired within the MIHST module. Such an approach is cost effective for on-line test application.
Two instruction generation modules, namely:
1>The OPCode Generation (OPCG) module, in charge of generating microprocessor instruction opcodes.
2> the OPErand Generation (OPEG) module, in charge of generating instruction operands. It may be replicated more than once, depending on the ISA of the processor under test (i.e., on the maximum number of operands of an instruction); this module implements the simple manipulations that may be applied to an operand within a loop, such as shift, increment, etc.
A Control Unit, managing the overall application flow in collaboration with the Bus Interface Unit. A Bus Interface Unit, reading and writing the system bus.
A Results Collection module, compressing the monitored address, data and control bus signals, is in charge of generating the test signature. This function is suitable to be implemented by a MISR module.
An optional Test Access Mechanism module, in charge of interfacing the MIHST unit with the Automatic Test Equipment in case the encoded instruction sequence has to be uploaded from the outside

V .EXPECTED TEST ANALYSIS

Comparison between normal and test mode

	MIHST approach	Original SBST
Fault Coverage	97.8%	97.8%
Application time(cc)	165	210
Test Program size(bytes)	17	248

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VI. CONCLUSION

The MHIST module can be treated as Intellectual property (IP), where they can be used to test the functionality of any processor without any modification to the original design of the processor. The Hardware based self-testing surely adds overhead to the design , because it comes with design itself but to test the during the online mode. Advantages of hardware self-testing surely decreases the time required to test a design and they do not utilize the processor memory to store the test result, which is indeed a land mark in saving processor memory, space and time.

REFERENCES

[1]. P. Bernardi, et al., "A functional test algorithm for the register forwarding and pipeline interlocking unit in pipelined microprocessors," in Proc. of the International Design & Test Symposium, Qatar, 2012, pp. 1-6.[2].
[2]. P. Bernardi, M. Grosso, E. Sanchez, and O. Ballan, "Fault grading of Software-Based Self-Test procedures for dependable automotive applications," in IEEE Design, Automation and Test in Europe,Grenoble, 2011, pp. 1-2.
[3]. P. Bernardi, et al., "On-Line Software-Based Self-Test of the Address Calculation Unit in RISC Processors," in Proc. of the European Test Symposium, Annecy, 2012, pp. 1-6.
[4]. K.Shimizu, D.L.Dill, A.J.Hu; "Monitor-Based Formal Specification of PCI"; Formal Methods in computer-Aided Design; Vol 1954 of LNCS; 2000; Austin, Texas. USA;Publisher Springer-Verlag; pp 335-352.
[5]. S.P.Luttik; "Description and Formal Specification of the Link Layer of P1394";Proceedings of the 2nd International Workshop on Applied Formal Methods in System Design; 1997; Editor I. Lovrek; pp 43-55.