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Design of a Low Power Flip-flop Using MTCMOS Technique in Cadence Tool

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***Abstract*- This paper enumerates low power, high speed design of Flip-Flops having less number of transistors and only one transistor being clocked by short pulse train which is true single phase clocking (TSPC) Flip-Flop. MTCMOS is one of the most important low power techniques which effectively reduce the leakage power. The MTCMOS operates in two modes – high threshold and low threshold modes. The high threshold mode reduces the leakage power and low threshold mode improves the speed performance. To reduce leakage power in MTCMOS circuits, sleep and sleep bar transistors are operated with high threshold voltages. When sleep input is OFF and sleep bar input is ON, there is no current flow in the low threshold voltage main circuit. When sleep is ON and sleep bar is OFF then the circuit works in normal Mode. The D Flip-Flop is simulated in 180nm technology using Cadence tool.**

***Keywords*- D Flip-flop, CMOS Technology, MTCMOS Technique, Cadence tool.**

I. INTRODUCTION

Flip-Flop is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. Flip-flops are often used in computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period sufficient for other circuits within a system to further process data [1]. At each rising or falling edge of a clock signal, the data stored in a set of Flip-Flops is readily available so that it can be applied as inputs to other combinational or sequential circuitry. Such flip-flops that store data on both the leading edge and the trailing edge of a clock pulse are referred to as double-edge triggered Flip-Flops Otherwise it is called as single edge triggered Flip-Flops.

Multi-threshold CMOS (MTCMOS) technology provides low leakage and high performance operation by utilizing high speed, low Vt transistors for logic cells and low leakage, high Vt devices as sleep transistors. Sleep transistors disconnect logic cells from the power supply and/or ground to reduce the leakage in sleep mode. In this technology, also called power gating, wake up latency and power plane integrity are key concerns. Assuming a sleep/wake up signal provided from a power management unit, an important issue is to minimize the time required to turn on the circuit upon receiving the wake up signal since the length of wake up time can affect the overall performance of the VLSI circuit. Furthermore, the large current flowing to ground when sleep transistors are turned on can become a major source of noise on the power distribution network, which can in turn adversely impact the performance and/or functionality of the other parts of the circuit. There is trade off between the amount of current flowing to ground and the transition time from the sleep mode to the active mode.

II. MTCMOS TECHNIQUE

Supply and threshold voltages are reduced with the scaling of CMOS technologies. Lowering of threshold voltages leads to an exponential increase in the sub threshold leakage current. In modern high performance integrated circuits (ICs), more than 40% of the total active mode energy can be dissipated due to the leakage currents. With more transistors integrated on-die, leakage currents will soon dominate the total energy consumption of high performance ICs. A popular low leakage circuit technique is the Multithreshold Voltage CMOS (MTCMOS).

The multi threshold CMOS technology has two main features. First, "active" and "sleep" operational modes are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages are used for N channel and P channel MOSFET in a single chip. This technique based on disconnecting the low threshold voltage (low-Vt) logic gates from the power supply and the ground line via cut-off high threshold voltage (high-Vt) sleep transistors is also known as "power gating". The schematic of power gating technique using MTCMOS is shown in Fig.1.The transistors having low threshold voltage are used to implement the logic. The transistors having high threshold voltage are used to isolate the low threshold voltage transistors from supply and ground during standby (sleep) mode to prevent leakage dissipation. In the active mode, sleep transistors are turned on and the logic consisting of low *VT* transistors can operate with high speed and low switching power dissipation. When the circuit is in sleep mode the high *VT* transistors are turned off causing isolation of low *VT* transistor from supply voltage and ground thereby reducing sub-threshold leakage current. The MTCMOS technique based

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D Flip-flop is shown in Fig.2. Fig.3.shows the schematic of MTCMOS based D Flip-flop in Cadence Tool.

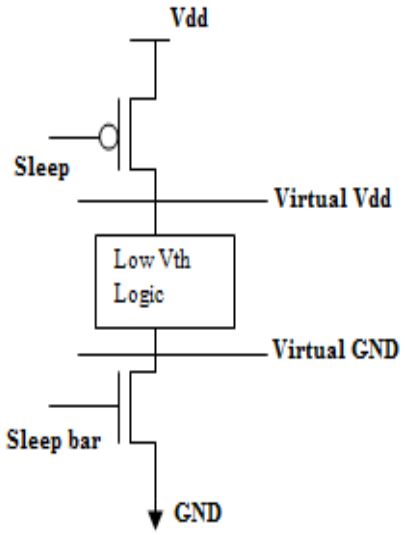


Fig.1.Power Gating Technique using MTCMOS

Table 1: MTCMOS based D Flip-flop

CLK	IN	Sleep	M1	M2	M3	M4	M5	M6	M7	OUT
0	0	0	on	On	Off	Off	On	On	Off	0
0	0	1	on	On	Off	Off	Off	Off	On	0
1	1	0	off	On	On	On	Off	On	Off	1
1	1	1	off	on	on	on	off	off	on	1

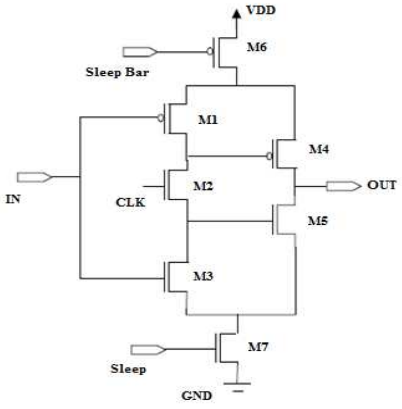


Fig.2. MTCMOS D flip-flop

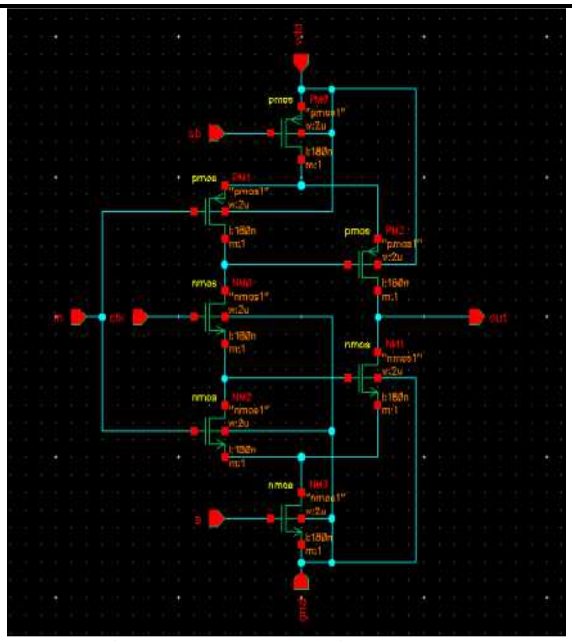
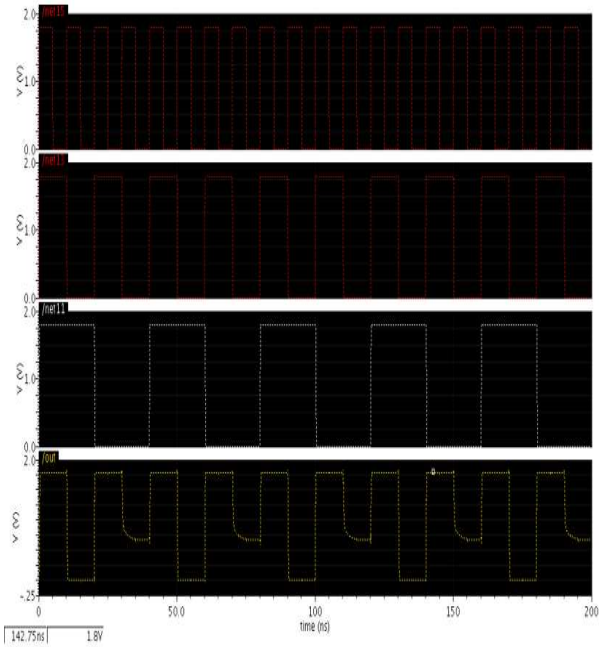


Fig.3. Schematic of MTCMOS based D Flip-flop in Cadence Tool

III. SIMULATION RESULTS



IV. CONCLUSION

This paper concludes that MTCMOS D Flip-Flop designed with 7 Transistors is having less power consumption. The D Flip-Flop is simulated in 180nm technology using Cadence tool. The circuits designed using MTCMOS are suitable for high performance applications like level converters, microprocessors, clocking systems counters, etc.

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REFERENCES

[1]. B. Chinnarao, B.Francis and Y.Apparao " Design of a low power flip-flop using CMOS deep submicron technology" ICEEE Sep, 2012.
[2]. M. A. Hernandez and M. L. Aranda, "A Clock Gated Pulse – Triggered D Flip-Flop For Low Power High Performance VLSI Synchronous Systems," Proceedings of the 6th International Caribben Conference on devices, circuits and systems, Mexico, Apr. 26-28, 2006
[3]. J.S. Wang, P.H. Yang "A Pulse Triggered TSPC FF for high speed, low power VLSI design applications" IEEE, 1998.
[4]. A. Keshavarzi, K. Roy, and C. F. Hawkins, "Intrinsic leakage in low power deep submicron CMOS ics," in Proc. Int. Test Conf., pp. 146–155, 1997.
[5]. J.T. Kao et al., "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits," IEEE J. Solid-State Circuits, vol. 35, no. 7, pp. 1009-1018, July 2000.
[6]. N. Sirisantana, L. Wei, and K. Roy, "High- Performance Low-Power CMOS Circuits Using Multiple Channel Length and Multiple Oxide Thickness," Proc. Int'l Conf. Computer Design (ICCD '00), IEEE CS Press, pp. 227-234, 2000.