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Design and Implementation of High Speed Application in the Field of PHM on FPGA

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***Abstract*-With the extensive application of new types of sensors, the rate of data acquisition and transmission are becoming a problem in Prognostic and Health Management(PHM). This paper presents an FPGA-based method for high speed data acquisition and transmission taking full advantage of the parallel processing capabilities and easy to modify and upgrade features of FPGA, to cope with the difficulties of high-speed data acquisition and transmission. This paper focuses on the components, performance and characteristics of the FPGA based fault prediction and diagnosis system. The system uses an FPGA chip as the core operational component to achieve fast transfer of large amounts of data by FIFO. The use of programmable FPGA hardware, makes the data acquisition system design flexible, while improving the reliability of the system. It is also important for achieving the real-time online monitoring of failure.**

Keywords- ADC; PHM; FPGA; FIFO; high-speed data transmission

I. INTRODUCTION

PHM seeks to use as few sensors as possible to collect data in order to evaluate the health status of a system using intelligent reasoning algorithms (such as physical model, neural network, data fusion, fuzzy logic, expert system, etc.).PHM applications can make fault forecasts before the occurrence of system fault, and provide a series of maintenance supporting measures to realize the condition based maintenance of the system with the use of all kinds of available resources. Fault diagnosis is an important prerequisite for the realization of healthy forecasts. In order to perform fault diagnosis, data acquisition and transmission are a key first step for any PHM system. So the advanced data acquisition system is the foundation for the development of PHM technology. With the wide application of various new sensors, data acquisition and transmission speed becomes a big problem restricting fault prediction and diagnosis. For example, ultrasonic testing has the advantage of requiring simple equipment and being, easy and safe to use, with a wide testing range. This has resulted in it becoming commonly used testing method in the field of Machinery manufacturing, petrochemical, aerospace and so on. Ultrasonic echo signal is a high frequency signal with frequency generally between 0.5 to 10 MHz. For example, the ultrasonic signal center frequency for rail examination reaches 2.5 MHz. To make such high frequency signal digitization, the system will put forward high requirements on module /digital switching circuit. According to Shan-non sampling theorem and Nyquist sampling standards, in order for the Digital samples to reproduce the input signal without any distortion ,the sampling frequency shall be higher than 2 times the ultrasonic signal frequency. In order to improve the signal-to-noise ratio,the testing precision, and to better draw the measured waveform, over-sampling technology beyond the Nyquist sampling rate shall be applied. Therefore, the sample rate of the whole system will be determined as 100 MHz. Obviously, the traditional acquisition system cannot meet the requirement of such high speed signal acquisition.

Aiming at the difficulties of fault diagnosis and health management technology in high speed data acquisition and transmission field, this paper makes full use of the parallel processing capability of FPGA as well as the characteristics of Programmable Logic Device-easy to modify and update to put forward the FPGA technology-oriented fault prediction and diagnosis method based on the synchronicity and quickness of the fault diagnosis system.

Of course, in order to meet the needs of different testing requirements, the sampling rate for the system can be adjusted. We can reduce the sampling rate to reduce the buffer capacity requirements when the testing frequency is not very high.

II. GENERAL DESIGN

The sampling frequency of the proposed design can reach as high as 100 MHz, however the host computer system can't be directly involved in data transmission due to the restrictions on operation speed. Therefore, this design employs a processing register as buffer storage between the high-speed AID converter and the microcomputer. The high-speed data acquisition system diagram is shown in figure 1. When the analog signal is digitized through the high-speed AID converter, it will be directly sent to the cache region. Then the stored data will be sent to the microcomputers for related processing and operating. Among which, cache region FIFO (First in First Out) becomes the indispensable component to solve the reliable transmission problem of cross clock domain data. It receives the data digitized by the AID converter at high speed, and then sends the data to the computer at lower speed to solve the contradiction between the high-speed AID conversion and low-speed computer data transmission in form of "Quick in Slow Out".

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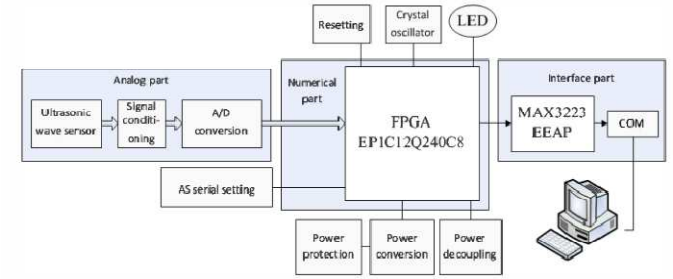

Figure 1. The general scheme of the system

III. ANALOG PART

AD9433 is a 12-digtal monolithic sampling AID converter, from the simulator company. It is endowed with chip tracking \ retaining circuit, and it will make the design more practical and more convenient. The conversion rate of the product is as high as 125 MSPS, and the optimization design is made for outstanding dynamic performance suitable for broadband and high IF carrier systems.

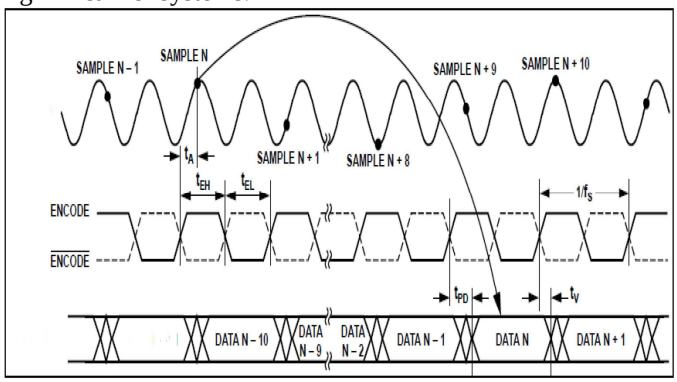

Figure 2. Timing sequence diagram of AD9433

IV. NUMERICAL PART

A. *Function overview of FPGA*

The FPGA is the core module of the design, containing the digital circuit. In the design process, the SOC (system on chip) concept is utilized. All the digital logic needed in the system is realized by the FPGA, including flip-flop, memory buffers, PLL, counter, serial interface logic, etc. The numerical part of the system can be fully programmable and adjustable by programming the FPGA according to the demand so that it has strong adaptability and flexibility. Based on the above ideas, this paper has chosen EPICI2Q240C8, a type of Cyclone from Altera Company and the design simulation is performed with the use of Quartusll development platform.

The functions completed by FPGA can be described as follows:

1. Introduce the external signal source clock into the FPGA, and make the corresponding frequency multiplication and fractional frequency processing through its internal PLL;
2. Output the clocks needed by the external AD9433 and RS232 bus into AD9433 and RS232 bus interfaces respectively through design clock output logic module, according to the operation situation;
3. Conduct the isolation treatment among different clock domains through its internal FIFO, introduce data has been acquired by AD9433 and synchronize to the FPGA internal clock domain, and then perform follow-up forwarding treatment;
4. Convert the data after buffering into standard message format and then send to the serial interface through the design data sending module.

B. *Data cache of FIFO*

FIFO (First in First Out) is a kind of First in First Out data buffer, where the data is stored into the FIFO input interface and then is sent out from the output interface of the FIFO in the same order. Therefore, the write and read of data in FIFO will only be controlled by the read/write clock and read/write request signal, it doesn't need the read/write address line.

There are two main roles with FIFO: 1. The FIFO acts as the data buffer for data transmission among different clock domains. 2. It realizes the purpose of data matching by FIFO as to data interface with different data width. In this design, both the two roles are reflected. Due to the higher sampling frequency in the design, which is about 100 MHz. Serial communications can hardly meet the requirement so it needs to use the FIFO buffer as a data cache to convert high-speed data flow into low-speed data flow meeting the requirements of RS232 communications. And because the AD9433 output is 12-bit data of the chosen AD conversion, the data sent to COM should be 8-bit, so another FIFO is needed to realize data matching.

This design will be completed with the basic macroblock in the development tool of Altera in Quartus II. The basic macroblocks of Altera are all optimized. They are used in the design of specific Altera device and can often accommodate users with higher design requirements and fewer resources and greatly reduce the development cycle. In order to invoke the FIFO module through the Mega Wizard manager, it needs to establish relevant parameters. These parameters include data width (THE WIDTH) and data depth (THE DEEPTH). Data width is the digital data of one FIFO data operation. Data depth reveals how many N-digital data (if the width is N) the FIFO can store.

The following includes the parameter settings to the two FIFO modules in the design, the logical principle diagram and the function simulation waveform.

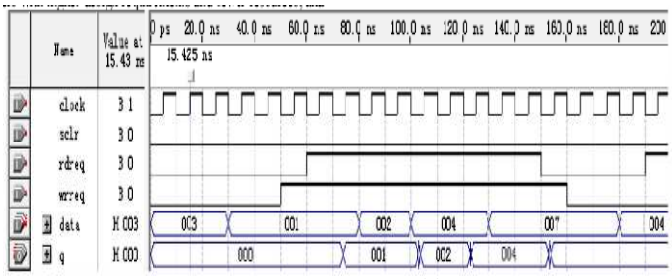

Figure 3. Timing sequence simulation of former-stage FIFO

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1. Former-stage FIFO

The FIFO is the first stage caching where the data is converted by the AID converter. Its main effect is to convert high-speed data into low-speed one. The width of FIFO is set as 12 bits and depth 1024 words.

The timing sequence simulation chart is shown in figure 3.Do_ad [11... 0] is the output of the A/D converter, and acts as data input of the ADFIFO module. Clock acts as the reading and writing clock signal of the ADFIFO. Sclr is the asynchronous reset input signal of ADFIFO and is effective when the high level signal is received. Wrreq is the write enabling signal of ADFIFO, and is effective when the high level signal is received. Rdreq is the read enabling signal of FIFO, and is effective when the high level signal is received. The data output port q [11... 0] of the ADFIFO works as the input of the last-stage FIFO (COMFIFO). The write full signal (wrfull) and read empty signal (rdempty) represent the present FIFO data depth. When the wrfull detects high electricity, the data in FIFO is in the full state and it is not allowed to write more data in the FIFO. But, when rdempty detects high electricity, there is no data in FIFO, and it is not allowed to read data out. If it is forced to read data, the data will be repeated out.

2. The last-stage FIFO

The FIFO is the second stage caching, and its main function is to convert the 12-bit data into two 8-digital data so as to realize the matching with the serial communication protocol. The FIFO width is set to 8 bits with a depth of 2048 words.

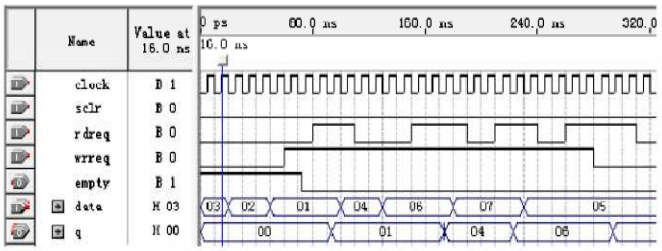

Figure 4. Timing sequence simulation of latter-stage FIFO

The interface definitions of the FIFO and the former-stage FIFO are similar to each other, so this paper will not give further description on them. In addition, this design takes rdempty as the input signal of the reading and counting module so as to read out data from COMFIFO if the state of COM FIFO is not empty.

B. Reading and writing control modules

In the digital system design, if it intends to perform a control function, we usually choose FSM (Finite State Machine) or CPU. As for the use of CPU, the execution speed is related to the CPU operation speed and specific coding style; if it is to use the FSM, the execution speed is mainly affected by the needed time for update the new state. Practice shows that in regards to execution time and the certainty of execution time, FSM performs better than the CPU.

FSM has two roles: one is to make decision on the command the module module so as to make it conduct the appropriate operation at the appropriate time. The other role us is to coordinate the timing sequence relation of the modules. The work of FSM is divided into two steps: the first step is to calculate the next state and the second step is to write into a new state register.

This design chooses a Moore FSM with eight kinds of states (SO ~ S7). The change of the state will be determined and realized by the control output of the corresponding state according to the AD data size as well as the full and empty condition of the FIFO. Each state's input/output are shown in figure 5:

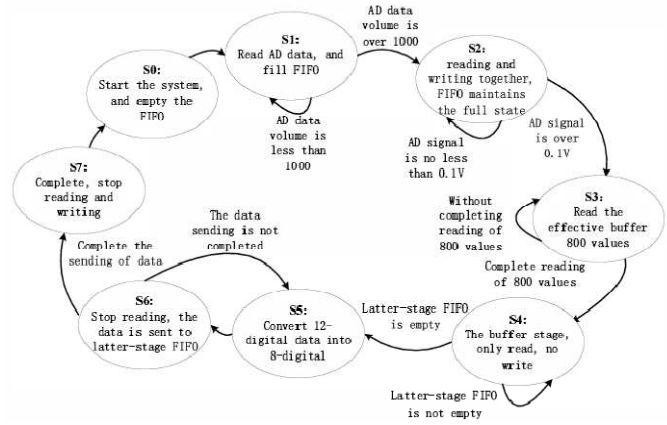

Figure 5. State transition chart of reading and writing control module

SO: the system is started. Empty the former-stage FIFO and counters reset. After one hour, the state will jump to the S 1 automatically an hour later.

S1: set the write enabling of the former-stage FIFO as 1, read the AD data, and start counting. When the read AD data volume is more than 1000, jump to S2. If not, it will still be in S1 in the following hour.

S2: wait for effective AD data. Both the former-stage FIFO reading and writing enabling data are set as 1, reading and writing together. When voltage signal of 0.1 V is found, or there are more than 256 data volume signals, jump to S3. If not, it will still be in S2 in the following hour.

S3: both read and write enabling of the former-stage FIFO is set as 1. Read the effective AD data. When the data volume reaches 800, jump to S4. If not, it will still be in S3 in the following hour.

S4: buffer stage, both read and write enabling of the former-stage FIFO is set as O. The write enabling of the latter stage FIFO is set as 0 with counters reset. When the latter-stage FIFO is empty, it will jump to S5. If the latter-stage FIFO is not null, it will still be in S4 in the following hour.

S5: read enabling of the former-stage FIFO is set as 1. The write enabling of the latter-stage FIFO is set as 1. Add the 2-digital "00" before the first 6-digital of the 12-digital data, then write into latter-stage FIFO, also begin to count. The state will jump to the S6 automatically an hour later.

S6: read enabling of the former-stage FIFO is set as O. The write enabling of the latter-stage FIFO is set as 1. Add the 2-digital "10" before the first 6-digital of the 12-digital data, then write into latter stage FIFO. If the data volume that has been sent is over 1000, jump to S7. If not, jump to S5.

S7: read enabling of the former-stage FIFO is set as O. The write enabling of the latter-stage FIFO is set as O. End the buffer cycle. And it will jump to SO one hour later.
In other states, it will jump to SO one hour later.

C. Data transmission module

The data transmission module is responsible for reading the data from the FIFO after processing, sending it to MAX232 to complete the level translation, and then return to PC to analyze. This is to prove whether the data after confirmation and processing is in accordance with the requirements of the design. UART provides read enabling signal re_comfifo to COMFIFO. After data processing units complete coding a number, the effective value will be stored. Then the re_comfifo will be taken as the high extraction memory data. Now, the data of COMFIFO can be converted into eight-digit. The data to be sent to PC shall conform to the standards of the synchronized serial port communication. Therefore, the eight-digit data output from FIFO shall be added with start bit and stop bit so as to realize the data transmission function.

V. RESULT DISPLAY

This design uses MFC to compile a PC interface, and display the detected waveform. After verification, it can detect the changes and the conditions of the waveform that result from material defects. Further analysis of data can be made on the acquired data and waveform with the use of Matlab so as to service for fault diagnosis and health management expert system.

VI. CONCLUSIONS

This paper introduces the components of the system, performance and characteristics of a fault diagnosis and prediction device based on FPGA, It conducts a detailed introduction of the system structure and design ideas of the FIFO data cache.It also gives the design process of FPGA internal timing sequential circuits with a logic principle diagram and simulation timing sequence diagram. It tests the feasibility of the overall design through experimental results. This system takes FPGA chip as the core operation components, and conducts fast transmission of large amounts of data through FIFO type RAM composed of FPGA. It makes use of the programmable characteristic of the FPGA hardware to make the software and hardware design of the whole data acquisition system flexible and improve the reliability of system. Therefore, it is of great significance to on-line and real-time monitoring of faults.

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