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Design and implementation of a Multiplier-Less VLSI Architecture using Wavelet Filter Banks

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Abstract— **Wavelet based signal processing incorporating Hilbert transform pair is proved to be more efficient by many authors. The multiplier-less VLSI based architecture of wavelet filter bank for biomedical applications is being proposed in this project. The proposed architecture reduces the computational complexity and improves the performance by combining DWT, Hilbert transform and sampling. Multiplication is replaced by distributed arithmetic algorithm to achieve better performance.ECG signal analysis is done using wavelet filter bank. The VHDL is used as the hardware description language and the simulation is to be accomplished using Modelsim and Matlab simulator.**

Keywords—**Wavelet Filter Banks, Distributed Arithmetic, Hilbert transform, Multiplier less**

I. INTRODUCTION

The dual-tree complex wavelet transform (DTCWT) had become an attractive signal processing tool since it was proposed by Kingsbury [1, 2]. It overcomes the main drawbacks of real discrete wavelet transform (DWT), such as shift sensitivity and poor directional selectivity (in the case of multidimensional DWT). A pair of filter banks is used in DTCWT, with which the wavelet bases associated form (approximate) Hilbert transform pairs. This property is critical since it is vital to reduce shift sensitivity and improve directionality.

Two-channel filter banks can be classified into three types: Quadrature mirror filter banks, orthogonal filter banks and biorthogonal filter banks. For FIR filters, output is a linear convolution of filter coefficients and inputs. For an Nth-order FIR filter, the generation of each output sample takes N+1 multiply accumulate (MAC) operations. Multiplication is strongest operation because it is repeated addition. It require large portion of chip area. Power consumption is more. Memory-based structures are more regular compared with the multiply accumulate structures; and have many other advantages, e.g., greater potential for high throughput and reduced-latency implementation and are expected to have less dynamic power consumption due to less switching activities for memory-read operations compared to the conventional multipliers. Memory based structures are well-suited for many digital signal processing (DSP) algorithms, which involve multiplication with a fixed set of coefficients. Since multiplier is costly in terms of area, many multiplier centric techniques are developed for implementation of FIR filter to resolve this issue. FIR filter implementation is divided into two broad categories, one by the use of multiplier, can categorized as Multipliered FIR filter and another, without use of multiplier as Multiplier less FIR filter. In multipliered FIR filters, the efforts are taken to reduce the area either by sharing of multipliers or by manipulating the coefficients so as to reduce the number of multiplications, where as in multiplier less FIR filters, coefficient are transformed to other numeric representations whose hardware implementation or arithmetic manipulation is more efficient than the traditional binary representation. For this Distributed Arithmetic (DA) architecture used in FIR filter.

II. DA ALGORITHM

The "basic" DA technique is performed serially. The multiply and accumulate operation is rearranged bit-level by DA. ROM look-ups hides the explicit multiplications, which is an efficient technique to implement on Field Programmable Gate Arrays (FPGAs). The following expression represents a multiply and accumulate operation.

$$y = A_1 \times x_1 + A_2 \times x_2 + \cdots + A_K \times x_K$$

$$y = \sum_{k=1}^{K} A_k x_k \qquad \text{-------(1)}$$

Where A_k are fixed coefficients and
X_k are the input data words

Look-Up Tables (LUTs) are used to store pre-computed values of coefficient operations. These memory-based methods involve Constant Coefficient Multiplier method and the very-well known Distributed Arithmetic method as examples. Distributed Arithmetic (DA) algorithm appeared as a very efficient solution especially suited for LUT-based FPGA architectures. The paper presents the improvement and optimization of the DA algorithm aiming at the problems of the configuration in the coefficient of FIR filter, the storage resource and the calculating speed, which make the memory size smaller and the operation speed faster to improve the computational performance.

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b_{1n}	b_{2n}	b_{3n}	b_{4n}	contents
0	0	0	0	0
0	0	0	1	A_4
0	0	1	0	A_3
0	0	1	1	A_3+A_4
0	1	0	0	A_2
0	1	0	1	A_2+A_4
0	1	1	0	A_3+A_2
0	1	1	1	A_3+A_4+A_2
1	0	0	0	A_1
1	0	0	1	A_1+A_4
1	0	1	0	A_1+A_3
1	0	1	1	A_3+A_4+A_1
1	1	0	0	A_1+A_2
1	1	0	1	A_1+A_2+A_4
1	1	1	0	A_1+A_2+A_3
1	1	1	1	A_1+A_2+A_3 + A_4

Table.1 2^4 Word LUT of Data

III. WAVELET TRANSFORM USING FILTER BANKS

In digital signal processing the requirement arises to decompose signals into low and high frequency bands, after which it needs to be combined to reconstruct the original signal. Such an example is found in Sub-Band Coding (SBC). Perfect reconstruction of a two channel filter bank also known as the Quadrature Mirror Filter (QMF) Bank as it uses power complementary filters, is an example of it. Perfect reconstruction is a process by which a signal is completely recovered after being separated into its low frequencies and high frequencies.

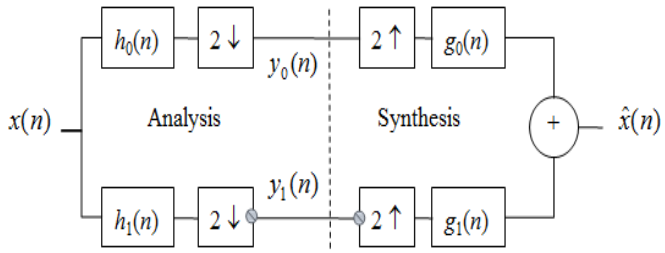

Figure1 QMF Filter Bank

A two-channel QMF bank shown in Figure 1, which is divided into analysis and synthesis section. The discrete input signal (n) splits into two subband signals having equal bandwidth, using the low-pass and high-pass analysis filters $h_0(n)$and $h_1(n)$ respectively. These signals are downsampled by a factor 2 at the transmitter end. At the receiver, the two subband signals are upsampled by a factor of two and finally passed through lowpass and high pass filters $g_0(n)$and $g_1(n)$ respectively. The outputs of the synthesis filters are combined to obtain the reconstructed signal $\tilde{x}(n)$.

Biorthogonal filter bank has proven quite useful for image processing .This name stems from the fact that $h_0(n)$ and $g_1(n)$ are orthogonal to each other and $h_1(n)$ and $g_0(n)$ are also orthogonal to each other. In biorthogonal context, the decomposition wavelet and reconstruction wavelets are designed in such a way that they forms Hilbert transform pair. From Figure 2 the decomposition wavelet ($h_0(n)$, $h_1(n)$) forms a Hilbert transform pair with reconstruction wavelet ($g_0(n)$, $g_1(n)$). For two orthogonal wavelets to form a Hilbert transform pair, the scaling filters (i.e. low pass filters) should be offset by a half sample.

$$h_0(n) = g_0(n - 1/2) \qquad \text{---------(2)}$$

IV. PROPOSED APPROACH

In this design methodology we have considered the input signal x(n) of 8 bits and utilized the same set of low pass and high pass filter coefficients as mentioned in [1].The rational scaling filter coefficients converted in to corresponding binary coefficients which are given in Table 2.

$h_0(n)$	$h_1(n)$	$g_0(n)$	$g_1(n)$
0.00000000	0.00000100	0.00000000	0.00000000
-0.00000010	-0.00000100	-0.00000100	0.00000000
0.00001100	-0.00100100	-0.00000100	0.00000010
0.01000010	0.01100100	0.00100100	0.00001100
0.01101000	-0.01100100	0.01100100	-0.01000010
0.01000010	0.00100100	0.01100100	0.01101000
0.00001100	0.00000100	0.00100100	-0.01000010
-0.00000010	-0.00000100	-0.00000100	0.00001100
0.00000000	0.00000000	-0.00000100	0.00000010

Table.2 2^4 Binary Equivalent Form of the Rational Scaling filter Coefficients.

The DA of FIR filter consists of Look Up Table (LUT), Shift registers and scaling accumulator. In DA all the cumulative partial product outcomes are precomputed and stored in a Look Up Table (LUT) which is addressed by the multiplier bits. A filter with N coefficients the LUT has 2N values.

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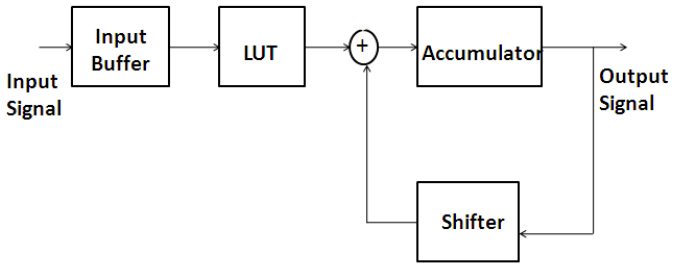

Figure 2 Basic architecture of distributed arithmetic

Each product term consists of a variable (signal) and a constant (coefficient) both in fixed point binary format but not necessarily of the same word length; Rather than compute the product on a term by term basis, the partial products of all terms are computed simultaneously, and in the time it would take to compute a single partial product on bit by bit basis. These partial products are generally the filter coefficients. These partial product filter coefficients of all terms are cumulated on bit by bit basis .Finally all the cumulative partial products of each bit are added and the result is produced.

In DA, all the cumulative partial product outcomes are precomputed and stored in a look up table which is addressed by the multiplier bits. All input variables are sequenced simultaneously.

A. Input Register

A stream of input samples x(n) of data width L stored in input registers. Converting these parallel formed input samples, into serial form, advanced to right for every clock, so as to create an address of LUT.

B. LUT Slicing

Exponential growth of single LUT can effectively be restricted by slicing the LUT into desired number. When k^{th} order LUT is divided into m slices, forms k units.

C. Accumulator and Shifter Unit

This stage consists of an accumulator and a shifter. The partial product generated by LUTs is added and shifted in every iteration. Number of iterations is defined by the input.

V. Conclusions

This paper proposes a novel VLSI design methodology of wavelet based Hilbert transform without the use of any multipliers. The design has been validated by implementing it on a Xilinx 14.1 version based FPGA using Virtex device. VHDL has been used as the HDL and ISIM as the simulator. The VLSI architecture implements Distributed Arithmetic, which has proved to be an area efficient, technique of FIR filter implementation.

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