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Design of low power SRAM using 5T in Cadence tool

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***Abstract*- This paper presents a 5-transistor SRAM cell intended for the advanced microprocessor cache market using 180nm CMOS technology. Semiconductor memories are most important subsystem of modern digital systems. In new era the scaling of silicon technology has been ongoing, due to scaling large memory can be fabricated on a single chip as results memories are capable to store and retrieve large amount of information at high speed. But due to high density, power dissipation gets increases and speed decreases. So there is need for the design of low power and high speed circuit in memory.**

Keywords- SRAM, CMOS Technology, Cadence tool.

I. INTRODUCTION

Due to the high demands on the portable products, energy consumption is a major concern in VLSI chip and microprocessor designs. The on-chip caches can effectively reduce the speed gap between the processor and main memory; almost modern microprocessors employ them to boost system performance. These on-chip caches are usually implemented using arrays of density packed SRAM cells for high performance. The purpose of this paper is to show that a SRAM cache memory can be designed using a 5T cell with smaller area than the 6T, while not sacrificing too much performance. Assuming that the 5T is functional, the area comparison is therefore the most important one.
The most apparent difference is that the 5T is asymmetric and almost square, whereas the 6T is symmetric and oblong. With the shared left-side contact the 5T has the same width as the 6T, but the height of the cell has been reduced by one total pass-transistor length.

We make the following key contributions:

1. Present a 5T bitcell with a novel asymmetric sizing approach to increase RSNM over an iso-area 6T.
2. Show how asymmetric sizing can be used as a knob to achieve an efficient trade-off between read delay, variability, area and leakage.
3. Demonstrate a functional 5T SRAM in a commercial 45nm bulk CMOS technology and analyze the pros and cons of a 5T relative to a 6T.Show measurements that confirm that the main problem With the 5T, writing a '1' can be overcome using write assist methods.
4. Demonstrate the scalability of the 5T bit cell.

SRAM is static random access memory in which used a 5 transistor to perform a read and write operation. It's a volatile in nature. To access a particular memory cell a 5T SRAM, the bit line and the word line must be activated. Once a memory cells are selected a data read and a data write operation have performed.

II. PROPOSED WORK

The read-write (R/W) memory circuits are designed to permit the writing and reading of data bits to be stored in the memory array. The memory circuit is said to be static if the stored data can be retained as long as a sufficient power supply voltage is provided without any need for a periodic refresh operation. The data storage cell or in other word the

1-bit memory cell in static Random access memory consists of a simple latch circuit with two stable operating states. Depending on the conserved state of the two-inverter latch circuit, the data being held in the memory cell will be interpreted either as logic "0" or as logic "1."

To access the data contained in the memory cell via the bit line, we need at least one switch, which is controlled by the corresponding word line, two complementary access switches consist of nMOS pass transistors are implemented to connect the 1-bit SRAM cell other word the 1-bit memory cell in static Random access memory consists of a simple latch circuit with two stable operating states.
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III. PROPOSED 5T SRAM CELL

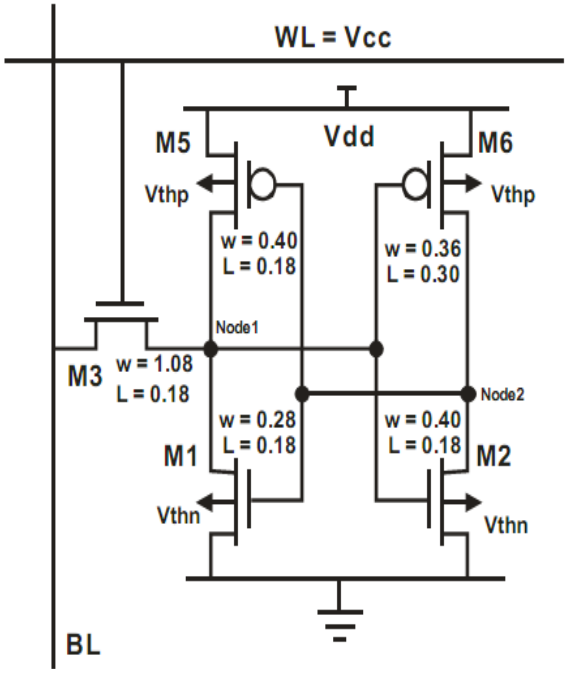
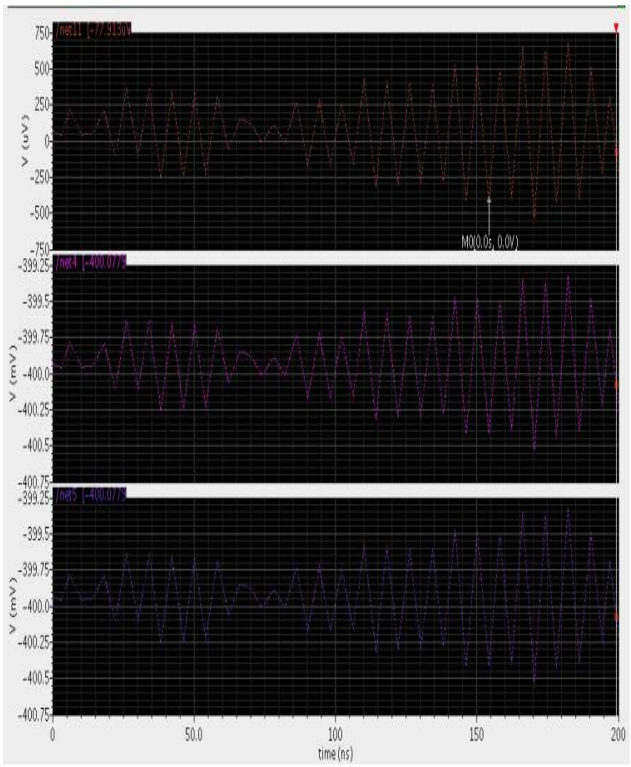


Fig 1. Block diagram of 5T SRAM CELL

The purpose of the proposed bit cell topology is to isolate the read and write operations from each other
and to eliminate the unnecessary two access transistors.
The first objective is accomplished by selectively controlling a closed-loop positive feedback gain, while the second objective is achieved by using a specialized controlling (timing) scheme that allows the inverter's driver or load transistor to behave as an access transistor under certain operating conditions. Fig 1. illustrates the proposed 5T schematic along with the timing scheme used to perform read or write operations.

Fig 1 shows the schematic of 5T SRAM in which used a three NMOS and two PMOS transistor. Which transistor is connected to word line
are called access transistor. With the help of these transistor controlling the bistable circuitry of SRAM. When bit line is activated and word line is low, no operation is performed by the circuit. When raising the word line of 5T SRAM the read and write operation is performed. Bit line basically a information.

IV. SIMULATION RESULTS



V. CONCLUSION

In this paper we presented a 5T SRAM with self controllable voltage level technique. The circuit structure and layout of Simulation is done by using a Cadence tool of 180nm CMOS technology. In this paper 5T SRAM design requires less area and less power compared to conventional 6T SRAM.

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