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High Resolution Synchronous DPWM technique on FPGA using IODELAY1 block

LINO M SAMUEL
Electronics department
The Oxford College of Engg, Bangalore
lino.msamuel@gmail.com

Mrs MEENA KV
Electronics department
The Oxford College of Engg, Bangalore

Mrs SAVITA Y PATIL
Electronics department
The Oxford College of Engg, Bangalore

Mrs SASIREKHA GVK
Electronics department
The Oxford College of Engg, Bangalore

***Abstract*—Digital Pulse Width modulation or DPWM techniques are used widely now a day in converters and other controlled applications because of its better stability and efficiency. In DPWM we use bits for determining the width of a PWM pulse so in controlled application as the resolution increases so as the control over that application. This paper proposes a DPWM technique using IODELAYE1 block in vertex6 FPGA for obtaining high resolution PWM signal.**

Keywords—DPWM, Resolution, Converters

I. INTRODUCTION

In modern world need of energy harvesting techniques is increasing day by day and the outputs from these techniques are non-predictable. So in order to stabilize the output we use power converters like DC-DC converter [8][9]. DIGITAL pulse-width modulators (DPWMs) have become a basic building block in digital control architectures of any power converter. The DPWM frequency is mainly determined by the power converter operating conditions, whereas the DPWM resolution determines the accuracy in the output voltage/current control.

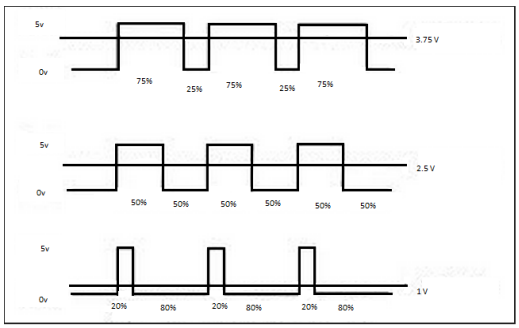

Fig.1. waveform showing control over voltage

As a consequence, the DPWM resolution has a direct impact in the power converter performance. Traditional DPWM implementations are based on counters and comparators, which generate the power converter gating signals according to several predefined thresholds. For these designs, the minimum on-time step is equal to the counter clock period. Its equivalent number of bits $\square_{DPWM}$ is

$$\square_{DPWM=} \log_2 (f_{clk} / f_{sw}) \qquad (1)$$

where f_{SW} is the DPWM frequency and f_{CLK} is the counter clock frequency. Nowadays, power converters are evolving toward designs with higher switching frequencies in order to reduce the size of inductors and capacitors. Besides, for the digital implementation, the number of bits $\square_{DPWM}$ has to be higher than the A/D converter resolution to avoid limit cycling. As a consequence, an unfeasibly high clock frequency can result, increasing the complexity and the cost of the final implementation.

Moreover, recent developments in semiconductor technology enable the use of higher switching frequencies through SiC and GaN power devices. This allows the design of power converters with reduced size and cost, and improved dynamic behaviour and power density, as shown in [3] and [4]. However, these designs require high-frequency high-resolution PWMs (HRPWMs) in order to take the most of the power converter.

Most of DPWM techniques by delaying the reset signal are not fully synchronous. Asynchronous circuits make harder to perform static timing analysis and can result in glitching since controlling the logic and routing delays in an FPGA is more difficult than in ASIC implementations.

Traditional designs of DPWM were based on the combination of counter and multiplexers. These designs often provide less bit resolution and jitter.

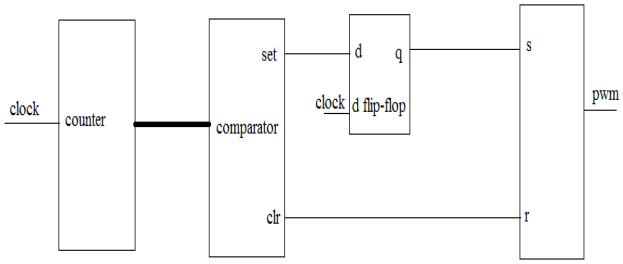

Fig.2 traditional design based on counter

A synchronous design, therefore, improves the reliability of the circuit and eases the design process. Besides, it makes the design more independent of the technology, easing the design portability.

In design is based on the I/O delay element (IODELAYE1) available in the Virtex-6 FPGAs or Virtex-7 FPGA's, and it provides higher resolution with a straight forward implementation.

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II. IODELAY1 ARCHITECHTURE

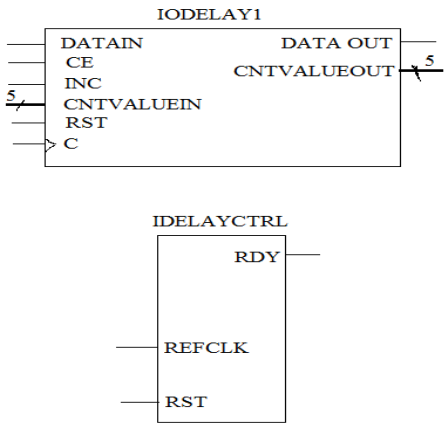

Fig.3. pinout description of IODELAY1 and IDELAYCTRL

The second approach uses the I/O delay element (IODELAYE1) [42] present in Virtex-6 series FPGAs or IODELAY2 present in Virtex-7 FPGAs. The IODELAYE1 block allows generating a signal (DATAOUT) delayed by a certain number of tap delays with respect to the input (DATAIN). The IODELAYE1 tap resolution is given by

$$t_{tap} = 1/(32 \cdot 2 \cdot f_{CK\_REF}) \qquad (2)$$

providing a fine delay-time t_d adjustment. The reference frequency f_{CK_REF} is set through the block attribute REF_CLK, and it can be either 200 ± 10 or 300 ± 10 MHz. Besides, it provides additional ports to configure the increment/decrement mode (CE), increment/decrement delay (INC), and reset (RST), which allows controlling the desired delay. These signals are synchronized with the clock signal C. When using the IODELAYE1 block, the IDELAYCTRL block must be also instantiated. This block continuously calibrates the delay elements in order to reduce the influence of process, voltage, and temperature variations by using the supplied REFCLK. Fig. 7 shows the pinout description of the IODELAYE1 and IDELAYCTRL blocks. The IODELAYE1 block offers three different operational modes when operating in the unidirectional input delay configuration, depending on the mechanism used to select the number of delay taps.

1) Fixed: The number of delay taps is predefined through the block attributes and it cannot be changed during operation.

2) Variable: The number of delay taps can be dynamically changed after configuration through the control signals CE and INC. When the enable increment/decrement signal (CE) is activated, the number of delay taps increases or decreases depending on whether the INC signal is activated or not. If the reset signal RST is activated, the delay value is reset to a predefined value.

3) Loadable variable: This mode has the same functionality as the variable mode. In addition to this, it allows loading the delay value through the 5-bit input CNTVALUEIN. When in this mode, the IODELAYE1 reset signal resets the delay value to a value set by the CNTVALUEIN. The delay time is, therefore, calculated as $t_d = t_{tap} \cdot$ CNTVALUEIN, and the current delay value can be read in the CNTVALUEOUT signal.

A. DPWM architecture using IODELAY1

Fig. 4 shows the proposed implementation for an m+1-bit HRPWM. Basically, the proposed circuit is made up of a synchronous m−4 bit counter, an IODELAYE1 block, two edge triggered flip-flops, an MMCM, and an SR latch whose output is the PWM signal. The difference of this design is that it replaces multiplexers from the traditional designs and uses IODELAYE1 block, making the implementation easier. Signals SETD and CLRD are generated comparing the counter output with zeros for SETD and the most m−5 significant bits of the duty command dc(m:5) for CLRD.

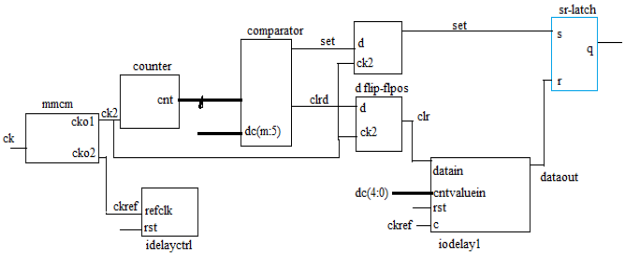

Fig.4.DPWM design using IODELAY1

For this implementation, the loadable variable mode for the IODELAYE1 block is used. The IODELAYE1 block delays the input signal through a 5-bit value CNTVALUEIN which can be updated when the RST signal is activated, which has to be synchronized with the C clock. Considering that the maximum 32-tap delay covers half a period of CK_REF, a clock that doubles the CK_REF frequency is required to clock the counter. These clock signals are generated through the MMCM using as a reference the board base clock CK.

The output frequency for the MMCM output i is set through its attributes M, D, and O as $f_{CKO} = M/(D \cdot O)$. In addition to this, the IDELAYCTRL is instantiated in order to auto calibrate the delay tap as previously explained.

Fig.5 shows the basic operation of the proposed IODELAYE1-based HRPWM architecture with dc =“10110100.” The CLRD signal is activated when dc(7:5) =CNT(7:5) = “101” = 4. The resulting pulse is captured in the next clock cycle by FFb, which generates the input signal for the IODELAYE1 block DATAIN. The IODELAYE1 block generates the RESET signal by delaying the CLR signal a number of tap cycles given by dc(4:0) = “10100” = 20. This signal clears the SR latch to generate the desired PWM signal.

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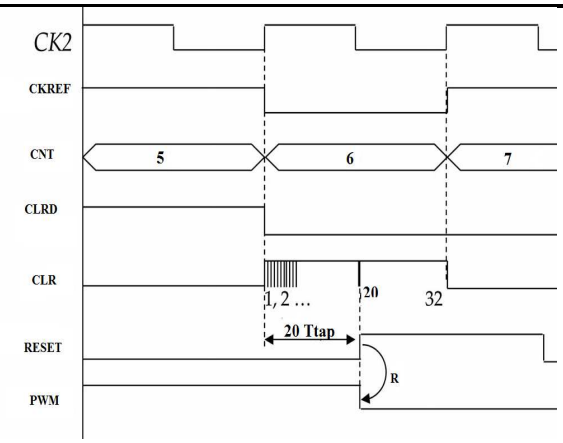

Fig.5. IODELAY1 operation for 10110100

B. *Synthesis*

The proposed IODELAYE1-based HRPWM architecture has been implemented in a Xilinx Virtex-6 XC6VLX240T- 1FFG1156 in the ML605 Evaluation Kit featuring a 200-MHz oscillator that is used as the input clock. The REF_CK clock frequency for the IODELAYE1 block has been set to 200 MHz, achieving a resolution

$t_{tap} = \Delta ton = (1/ (32 \cdot 2 \cdot f_{CKREF})) = 78$ ps.

Therefore, the CK2 clock frequency for the counter and the flip-flops is 400MHz. These clock signals are generated through the MMCM configured with M = 8,D = 2,O1 = 2, andO2 = 4. The proposed design can operate correctly with 32-bit counters, allowing generating up to 10-s-width pulses with 78-ps resolution.

Output Clock Summary

VCO Freq = 800.000 MHz

Output Clock	Port Name	Output Freq (MHz)	Phase (degrees)	Duty Cycle (%)	Pk-to-Pk Jitter (ps)	Phase Error (ps)
CLK_OUT1	CLK_OUT1	400.000	0.000	50.0	111.164	114.212
CLK_OUT2	CLK_OUT2	200.000	0.000	50.0	126.455	114.212

Fig.6. clock output from MMCM in Xilinx

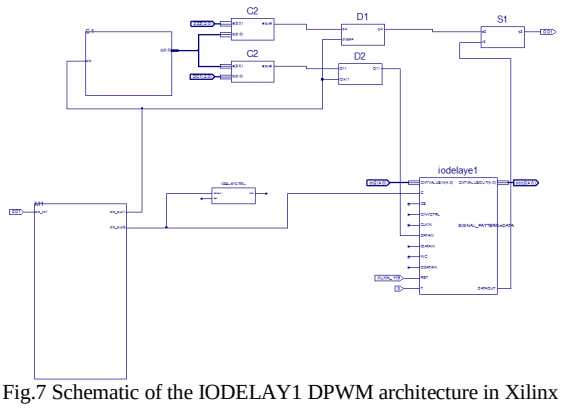

Fig.7 Schematic of the IODELAY1 DPWM architecture in Xilinx

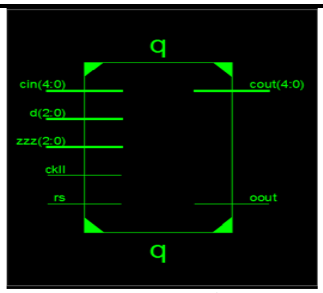

Fig.7 synthesis result of the design

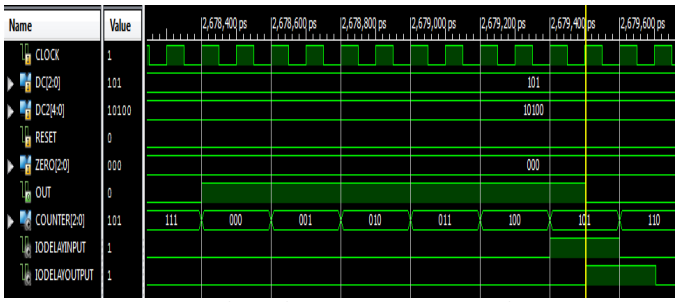

Fig.8.Output wave form of the DPWM architecture for 10110100

CONCLUSION

Advances in power electronics and digital control have made necessary the development of high-resolution DPWMs to take the most of either high-frequency or high-precision power converters. The IODELAYE1-based architecture are synchronous architectures have been designed on Virtex-6 FPGA comparing to designs in [1], [2], [5] and [6]gives better resolution. The IODELAYE1-based architecture offers a higher resolution and number of PWM outputs with a straightforward implementation using the high-end Virtex-6 FPGAs and cover a wide spectrum of cost/performance applications. The experimental results show a resolution 78 ps for the IODELAYE1-based architecture, showing the feasibility of the proposal.

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