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FPGA Implementation of 9 Port Router for 3D ON-Chip Communication using Verilog

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***Abstract*: The scaling of microchip technologies has enabled large scale systems-on-chip (SoC). Multiprocessor SoC is emerging as a new trend for System on chip design but the wire and power design constraints are forcing adoption of new design methodologies. For systems with intensive parallel communication requirements buses may not provide the required bandwidth, latency, and power consumption. A solution for such a communication bottleneck is the use of an embedded switching network called Network-on-Chip (NoC). In order to implement a competitive NOC architecture; the router should be efficiently designed as it is the central component of NOC architecture. In our paper we implement a NoC router which is designed for future 3D NoC architectures. This paper presents a work aimed to design the 9 port NoC Router modeled in Verilog and simulation results are shown in Questasim simulator and realized in Spartan-6 FPGA using Xilinx ISE 14.3i.**

***Keywords*—NoC, NoC router, Register, FSM, FIFO, Verilog**

1. INTRODUCTION

Nanometer technologies allow integration of millions of transistors on a single chip. As the integration goes on increasing it exacerbates the design productivity gap and timing closure problems. A system on chip is an integrated circuit that integrates all components of a computer or other electronics system into a single chip. The major challenge the designers of these systems must overcome is to provide functionally correct and reliable operations of the interacting components. On chip physical interconnections will present a limiting factor for performance and energy consumption [1].

Generally, bus is utilized for interconnecting the processing elements of System on Chip (SoC). However by increasing the number of processing elements, the bus itself is transmuted into a bottleneck. To obviate this difficulty, the idea of Network on Chip (NoC) has been introduced [2].
This network can be modeled as a graph wherein nodes, processing elements and edges are the connective links of the processing elements. In this article, designing and implementing NoC router are presented.

Figure 1 shows a sample NoC as a 3x3 mesh topology which provides global chip level communication. It shows the 2D mesh architecture. The processing element (PE) can be a general purpose processor, a DSP, an embedded memory etc. Each PE is attached to a router which connects it to its neighboring PEs. The X, Y indicates the 2-Dimensions/co-ordinates.

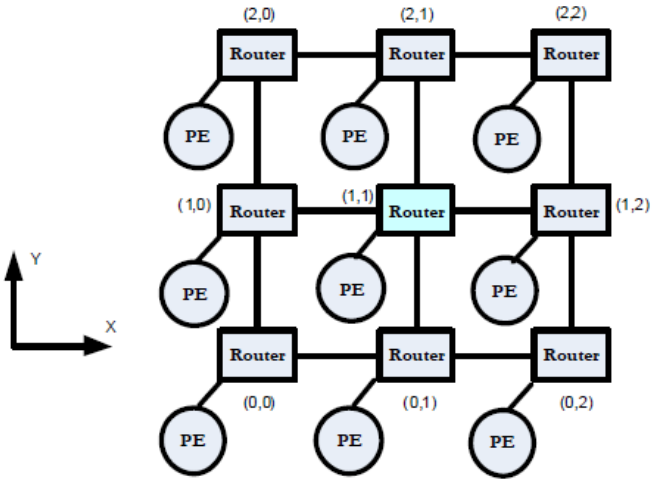

Fig-1; 3x3 mesh topology (2D mesh)

It is becoming clear that soc presents major technical, financial, business and legal challenges that are forcing industry and academic researchers to consider other options for semiconductors and systems. For the first time, "Industry may not invest in extending Moore's law beyond 2015".This is leading the industry to explore alternative ways to achieve systems integration where in semiconductor integration is pursued, not only horizontally by SoC, but also vertically by SIP via 3D stacking of bare or packaged ICs and by SOP.. Thus we require 3D-NoC architectures.
Three-dimensional integrated circuits (3D IC) refers to a stack consists of multiple ultra-thin layers of IC that are vertically bonded and interconnected with Through Silicon Via (TSV).
Enabling design in the vertical dimension permits a large degree of freedom in choosing an on-chip network topology.

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Due to wire-length constraints and layout complications, the more conventional two-dimensional integrated circuits have placed limitations on the types of network structures that are possible. With the advent of 3D ICs, a wide range of on-chip network structures that were not explored earlier are being considered.
The straightforward extension of this popular planar structure is the 3D Mesh. Figure 2 shows an example of 3D Mesh NoC. It employs 7-port switches: one port to the IP block.

In the future, new architectures shall be developed, and there is a requirement of a router with 9 ports, with 8-input output ports, and one local port connected the IP (or Processing Element).

Figure 3 shows the 2D and 3D structures of IP and Router (switch).

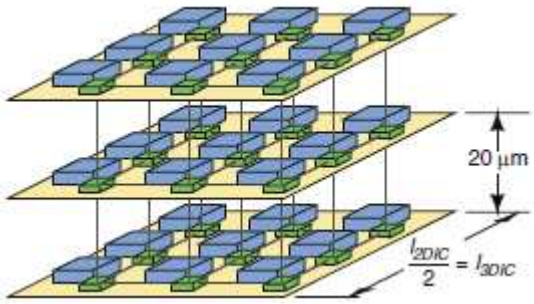

Fig- 2; 3D Mesh NoC

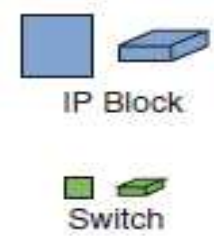

Fig-3; 2D and 3D IP block and Switch

2. RELATED WORKS

In this section, we discuss some literature analysis of various contributions to the NOC domain.

A. Topology

From the view of communication we know many topologies for NOC architecture. These include mesh, torus, ring, buttery, octagon and irregular interconnection networks [3], [4]. Various researchers have exploited these different NOC topologies for their NOC implementations.

- Adriahante naina et al. proposed a tree based implementation of NOC [5], where each node in the tree behaves as a router in NOC;
- Pande et al. compared various network topologies for interconnection networks in terms of latency, throughput, and energy dissipation [6].

B. ROUTER ARCHITECTURE

NOC architectures are based on packet-switching. It has led to efficient principles for design of routers for NOC [7]. Various designs and implementations of router architectures based on different routing strategies have been proposed in the literature

- Wolkotte et al. proposed a circuit switched router architecture for NOC [8] but Dally and Towels proposed a packet switched router architecture.

C. Routing protocol

Routing algorithms can also be defined based on their implementation: lookup table and Finite State Machine (FSM). Lookup table routing algorithms are more popular in implementing. They are executed in software, where a lookup table is stored in every node. FSM based routing algorithms may be designed either in software or in hardware.

- Mello et al. researched the performance of minimal routing protocol in NOC [9]. They concluded that the minimal routing provided better results than adaptive routing for on-chip communications, as the adaptive routing concentrates on the traffic in the center of the NOC.

D. Switching technique

The NoC switching strategy determines how data flows through the routers in the network. Switching techniques can be classified based on network characteristics. Circuit switched networks reserve a physical path before transmitting the data packets, while packet switched networks transmit the packets without reserving the entire path. Packet switched networks can further be classified as Wormhole, Store and Forward (S&F), and Virtual Cut Through Switching (VCT) networks (see Figure 2). In Wormhole switching networks, only the header flit experiences latency. Other flits belonging to the same packet simply follow the path taken by the header Switching Techniques Circuit Switching, Packet Switching Wormhole Switching, S&F Switching Virtual Cut Through flit. If the header flit is blocked then the entire packet is blocked. It does not require any buffering of the packet. Therefore, the size of the chip drastically reduces. However, the major drawback of this switching technique is a higher latency. Thus, it is not a suitable switching technique for real-time data transfers.

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- Al-Tawil et al. provided a well-structured survey of Wormhole Routing techniques and its comparison with other switching techniques [10]

3. PROPOSED WORK

The communication on network on chip is carried out by means of router. So for implementing better NOC, the router should be efficiently design. This router supports four parallel connections at the same time. It uses store and forward type of flow control and FSM Controller deterministic routing which improves the performance of router. The switching mechanism used here is packet switching which is generally used on network on chip.
In packet switching the data transfers in the form of packets between cooperating routers and independent routing decision is taken. The store and forward flow mechanism is best because it does not reserve channels and thus does not lead to idle physical channels. The arbiter is of rotating priority scheme so that every channel once get chance to transfer its data. In this router both input and output buffering is used so that congestion can be avoided at both sides.
A router is a device that forwards data packets across computer networks. Routers perform the data "traffic direction" functions on the Internet. A router is a microprocessor-controlled device that is connected to two or more data lines from different networks. When a data packet comes in on one of the lines, the router reads the address information in the packet to determine its ultimate destination. Then, using information in its routing table, it directs the packet to the next network on its journey.

"Nine **Port Network Router**" has one input port from which the packet enters and it has eight output ports where the packet is driven out. Packet contains 3 parts. They are Header, data and frame check sequence. Packet width is 8 bits and the length of the packet can be between 1 -64 bytes. Packet header contains three fields Destination address (DA) and length. Destination address (DA) of the packet is of 8 bits. The switch drives the packet to respective ports based on this destination address of the packets. Each output port has 8-bit unique port address. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the data is of 8 bits and from 0 to 63. Length is measured in terms of bytes. Data should be in terms of bytes and can take anything. Frame check sequence contains the security check of the packet. It is calculated over the header and data.

Router is a packet based protocol. Router drives the incoming packet which comes from the input port to output ports based on the address contained in the packet.
The router has one input port from which the packet enters. It has eight output ports where the packet is driven out. Figure 4 shows the block diagram of nine port router. The router has an active low synchronous input reset which resets the router. Data packet moves in to the input channel of one port of router by which it is forwarded to the output channel of other port. Each input channel and output channel has its own decoding logic which increases the performance of the router. Buffers are present at all ports to store the data temporarily.

The buffering method used here is store and forward. Control logic is present to make arbitration decisions. Thus communication is established between input and output ports. According to the destination path of data packet, control bit lines of FSM are set. The movement of data from source to destination is called switching mechanism The packet switching mechanism is used here, in which the flit size is 16 bits .Thus the packet size varies from 0 bits to 16 bits.

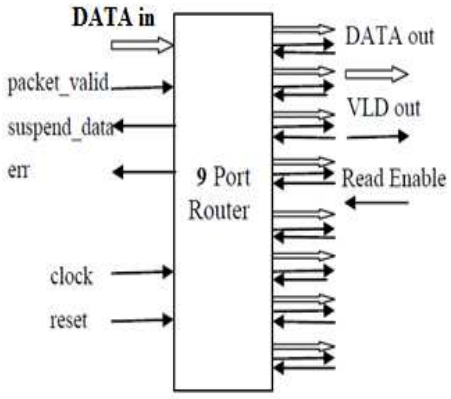

Fig-4; The block diagram of nine port router

Router internally consists of a Register, FSM and FIFOs at the input and output port. Fig 5 shows the internal structure of Router.

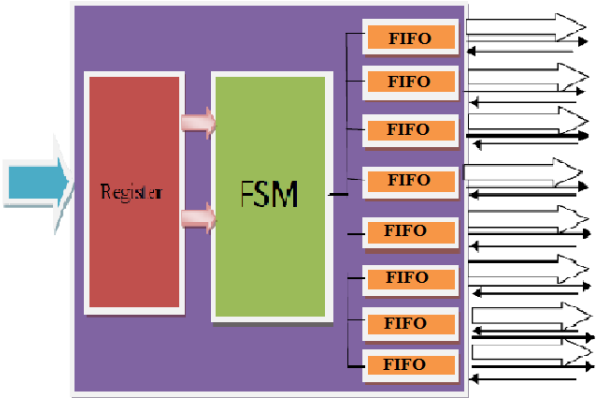

Fig-5; The internal structure of Router.

Register Block:

This module contains status, data and parity registers required by router. All the registers in this module are latched on rising

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edge of the clock. Data registers latches the data from data input based on state and status control signals, and this latched data is sent to the FIFO for storage. Apart from it, data is also latched into the parity registers for parity calculation and it is compared with the parity byte of the packet. Fig 6 shows the block of a register. An error signal is generated if packet parity is not equal to the calculated parity.

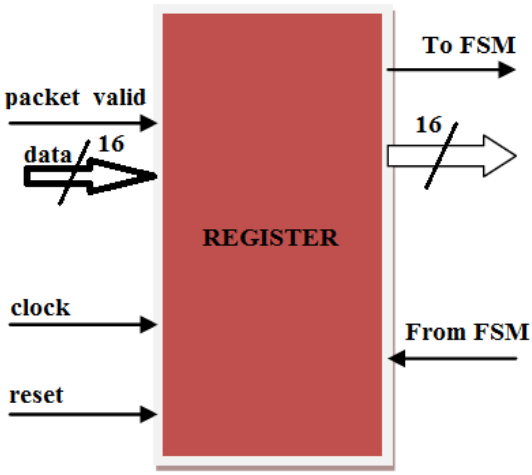

Fig-6; Register block

FSM block:

FSM acts as an arbiter. FSM is the heart of any Router. The arbiters are an important piece of the scheduler design in which Grant and request signals are identically designed with the exception of the rules determining when the Priority State may be updated An arbiter is required to share the resources among the many requesters. When putting an arbiter into a design, many factors must be considered. The interface between the requesters and the arbiter must be appropriate for the size and speed of the arbiter. Also, the coding style used will usually impact the synthesis results. Figure 7 shows the arbiter. The arbiter keeps away the system from metastability state of non arbitery system, when large number of request is sending from different clients to communicate with large number of resources. It works on three process request, grant and Accept

Step1 Request

Each unmatched input sends a request to every output which for which it has a queued cell.

Step2 Grant

In an unmatched output receives any requests, it chooses the one that appears next in a fixed, round-robin schedule starting from the highest priority element. The output notifies each input whether or not its request was granted. The pointer to the highest Priority element of the round-robin schedule is incremented (modulo N) to one location Beyond the granted input if the grant is accepted in Step 3 of the first iteration.

Step 3 Accept

If an unmatched input receives a grant, it accepts the one that appears next in a fixed, round-robin schedule starting from the highest priority element

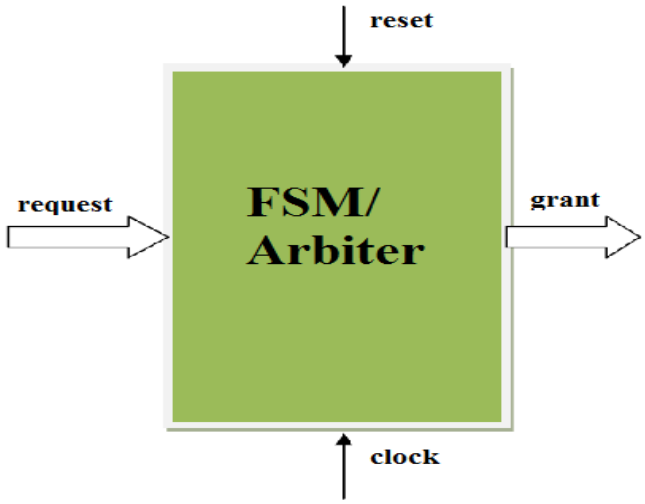

Fig-7; FSM/Arbiter

FIFO BLOCK;

There are 8 FIFOs used in the router design. Each FIFO is of 16 bit width and 16 bit depth. The FIFO works on system clock. It has synchronous input signal reset. If reset is low then fFIFO_full =0, fFIFO_empty = 1 and fread_data= 0
The FIFO has doing 7 deferent operations

- Write Operation
- Read operation

Read and Write Operation
The functionality of FIFO is explained below. Figure 8, Shows the FIFO block.

Write operation:

The FIFO write operation is done by when the data from input 'fwrite_data' is sampled at rising edge of the clock when input fwrite_enable is high and FIFO is not full. In this condition only FIFO Write operation is done.

Read Operation:

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In FIFO Read Operation, the data is read from output 'fread_data' at rising edge of the clock, when 'fwrite_enable' is low and FIFO is not empty.
Read and Write operation can be done simultaneously.
fFIFO_full– it indicates that all the locations inside FIFO has been written.
fFIFO_empty– it indicates that all the locations of FIFO are empty.

fFIFO_overflow- it indicates that FIFO is written and FIFO write address is greater than FIFO depth.
fFIFO_underflow- it indicates, FIFO write address is less than FIFO depth.

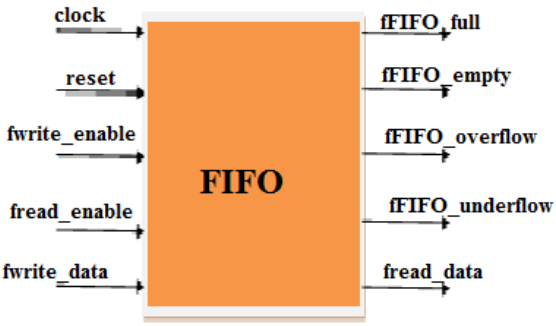

Fig -8; FIFO block

The output from the FIFO are given to the channels, these channels provide connections for the other PE. Thus the eight input-output ports provide connections for 8 other PE on the top stacked 2D IC layer, as well as with the bottom top stacked 2D IC layer. Hence the Router for 3D NoC architecture is developed.

4. SIMULATION RESULTS

In this paper, NoC Router is modeled in Verilog and simulation results are shown in Questasim simulator. Questasim simulator is provided by the Mentor graphics EDA tool developing company.

Firstly we shall observe the results of the FSM/Arbiter. The results are observed in the Wave window of the Questa sim simulator. For the Simulation of the FSM we have the signals for the request as r1, r2, r3, r4 and similarly for grant as g1, g2, g3, g4. Along with clock-clk, reset-rst, are observed in the wave window.fig 9 shows the simulation results of FSM Arbiter.

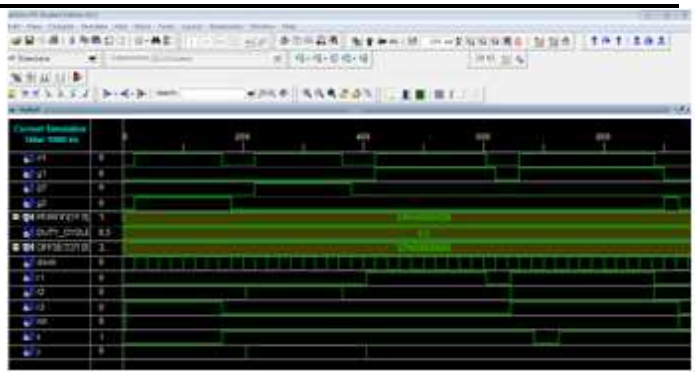

Fig-9; Simulation of FSM block

Next we observe the simulation of FIFO. The simulation result of write operation is as follows shown in figure 10.

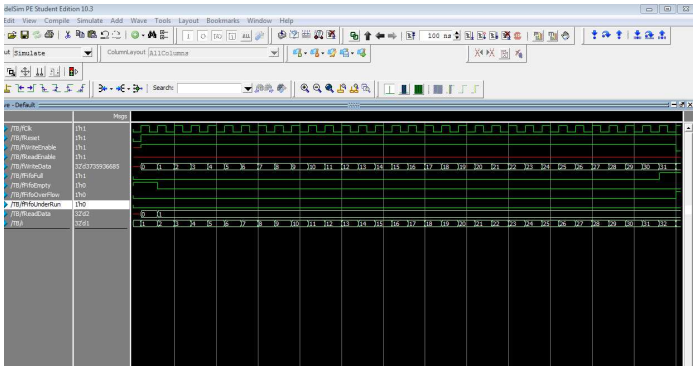

Fig-10; FIFO write operation

Similarly we simulate for read operation, figure 11 shows the FIFO read operation.

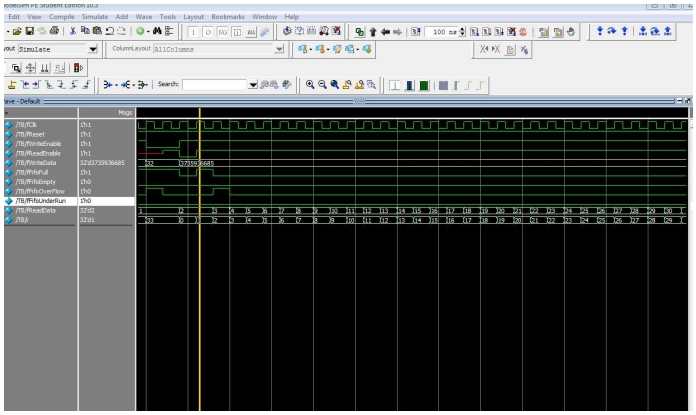

Fig-11; FIFO read operation

Finally the simulation result of the router is observed in wave window of Questasim as shown in the figure 12.

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5. CONCLUSION

In this paper, nine port NoC router of 3D NoC architecture is implemented using HDL called Verilog at RTL level. Architecture is synthesized using Xilinx14.1i and simulated using Questasim. The next step is to verify the design, which can be carried out using standard verification methodology, i.e. using UVM (Universal Verification Methodology)

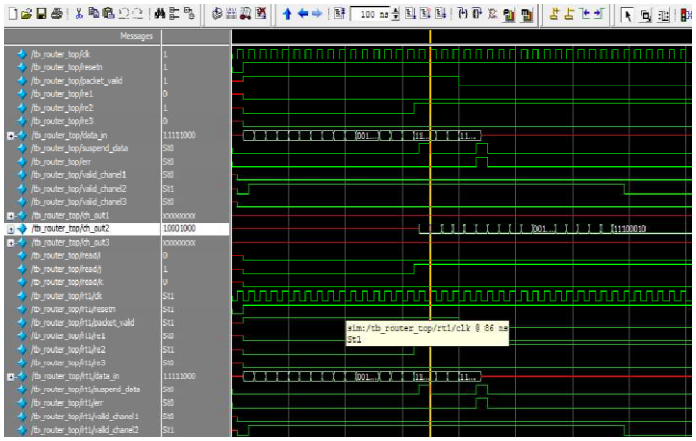

Fig-12; Simulation result of nine port Router.

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