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Design of Reliable Router Architecture Using Hamming Code Error Correction Techniques

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***Abstract*— In this project, a new reliable Network on Chip appropriate for dynamically reconfigurable Multiprocessors on Chip systems is designed and simulated. The suggested NoC design is based on routers accomplishing online error detection of routing algorithm and data packet errors. This project focuses on adaptive routing algorithms which allow bypassing faulty components or processor elements dynamically implemented inside the network. The intended routing error detection mechanism helps differentiate routing errors from bypasses of faulty components. The primary uniqueness in this NoC approach is that only the permanently faulty parts of the routers are disconnected. Hence, this approach results in high run time efficiency in the NoC without data packet loss due to the self-loopback mechanism inside each router.**

***Index Terms*— Network On Chip, Hamming Code, Router**

I. INTRODUCTION

Embedded systems with multiprocessor systems-on-chip (MPSoCs) is vastly increasing due to the needs of real-time applications. In such a scenario a communication fabric is needed which is scalable enough to handle the increasing performance requirements. Since the complexity of these system on chips is increasing in a vast rate, communication medium is experiencing lot of difficulties in MPSoC .The trademark of NoC medium characterizes a high level of modularity, flexibility, and throughput. A NoC consists of routers together with interconnections communicating between the PEs and IPs. The NoC depends on data packet exchange. In packet switching networks, routing directs packet forwarding (the transit of logically addressed network packets from their source toward their ultimate destination which is given by a routing algorithm) through intermediate nodes. Therefore, the path depends mainly on the flexibility and adaptively provided by the routing algorithm (partially or fully adaptive routing algorithm).

Dynamically reconfigurable 2-D mesh NoCs are most accepted for field programmable gate array (FPGA)-based systems. For achieving a reconfigurable NoC, a well-organized dynamic routing algorithm is required for the data packets. It should provide high NoC performance in terms of throughput while preserving flexibility and reliability. This paper describes a new reliable dynamic NoC which is a mesh structure of routers that are able to detect routing errors for adaptive routing of the *XY* algorithm. This approach includes data packet error detection and correction with Hamming codes. The originality of the proposed architecture is its ability to accurately detect error sources and thereby localizing, thus allowing the throughput and network load of the NoC maintained. The routing algorithm used here is based on the adaptive turn model routing scheme and the popular *XY* algorithm. This adaptive algorithm is free of livelocks and deadlocks, thus permitting data packets to go through faulty regions.

II. ARCHITECTURE AND DESIGN OF THE SWITCH

The switch has four directions (North, South, East, and west) needed for a 2-D mesh NoC. The processor elements can be connected directly to any side of a router and thus specific connection can be avoided. This mechanisms can be applied to NoCs using five port routers with a local port. It has two unidirectional data buses (input and output ports). Each input port has first-in first-out (FIFO) buffer and a routing logic block. The switching strategy used is the store-and-forward switching technique which is suitable for dynamically reconfigurable NoC. The type of error control method used here is automatic repeat request which uses error detecting codes, Ack/Nack solution which handles fault-tolerant transmissions effectively. Once a flit with an error fails to be corrected by ECC is detected by the neighboring router, a Nack is sent back and the whole packet is retransmitted. Otherwise, an Ack is sent by receiver indicating that full packet is being received correctly as a data frame as a result latency is reduced. The Hamming ECC is used here which provide a suitable tradeoff between area overhead and error correction capacity. Hamming code is more suitable for NoCs based on Ack/Nack flow control than the parity bit check. Indeed, hamming code can do error correction easily on a single bit-flip error occurrence, but in the case of single parity check it would need packet retransmission and thus would result in an increased transmission delay.

This reliable router switch architecture uses an online routing error detection process. The popular XY algorithm adaptive technique is considered here and that is being used for this routing algorithm. If a faulty node is present in the NoC, it would result in a permanent transient error, and that would result in a routing error. With the usage of adaptive algorithm, bypass of faulty component in the NoC can be done and this is the most difficult process in the routing error detection. This error detection challenge can be done by the reliable router switch. If the routing error is not detected properly, it would result in a huge data packet sequence

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latency, and as a result it would end up in a considerable loss of data packet sequence. If routing errors are not detected in time, in addition to raising the latency on the packet, the packets may wrongly be sent to a faulty router or to a block which is in the process of being configured and hence not fully ready to route the packets correctly. The basic idea of routing error detection is that each router that accepts the data packet sequence from the previously traversed switch will look for the accuracy of the routing decision. The error detection done by the router occurs in parallel after the Hamming code error detection is done. As a result, the latency of data packet sequence is not increased.

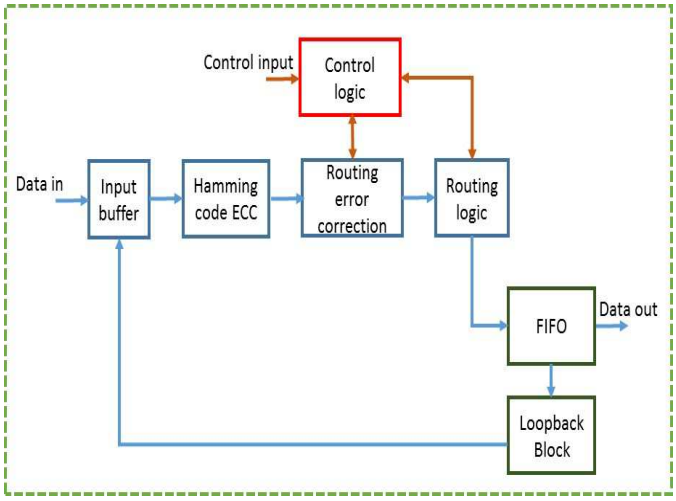

Fig 1. Architecture of one block of reliable switch

A. Designing (n, k, t) Hamming code

Forward error-correction coding also known as 'channel coding' is a method in digital signal processing which improves reliability of the data by the introduction of a known structure into the packet data before transmission. As the name suggests, this coding technique enables the decoder to correct errors without the need of requesting retransmission of the original content. Hamming code is most suited for forward error correction techniques. In a communication system that involves forward error-correction coding, the encoder receives the data sequence from the digital information source. The code word is formed as a result of insertion of redundant or parity bits by the encoder resulting in a longer sequence of code bits. Thus code words are then being transmitted to a receiver, where an appropriate decoder is used to extract the original data sequence. The (n, k, t) code refers to an 'n'-bit code word which has 'k' data bits (where n > k) and 'r' (=n–k) error-control bits implied as 'redundant' or 'redundancy' bits with the code correction capability of correcting 't' bits in the error (i.e. corrupted bits).If the total number of bits in the code word is 'n' (=k+r), 'r' should have the capability to indicate at least 'n+1' (=k+r+1) different states.

For example, a 7-bit ASCII code needs four redundancy bits which is added at the end of the packet data or distributed with the original packet data sequence bits to form the (11, 7, 1) Hamming code. These redundancy bits then occupy the position numbers 1, 2, 4 and 8 (the positions of an 11-bit sequence which has the powers of '2'). For ease of description in the examples below, these bits are labeled as 'R1,' 'R2,' 'R4' and 'R8'. In the Hamming code, parity bit is denoted by 'r' and the combination of data bits is shown below:

R1: 1, 3, 5, 7, 9, 11

R2: 2, 3, 6, 7, 10, 11

R4: 4, 5, 6, 7

R8: 8, 9, 10, 11

	11	10	9	8	7	6	5	4	3	2	1
Data	**1**	**0**	**0**		**1**	**1**	**0**		**1**		
R1	**11**	10	**9**	8	**7**	6	**5**	4	**3**	2	**1**
	1	**0**	**0**		**1**	**1**	**0**		**1**		**1**
R2	**11**	**10**	9	8	**7**	**6**	5	4	**3**	**2**	1
	1	**0**	**0**		**1**	**1**	**0**		**1**	**0**	**1**
R4	11	10	9	8	**7**	**6**	**5**	**4**	3	2	1
	1	**0**	**0**		**1**	**1**	**0**	**0**	**1**	**0**	**1**
R8	**11**	**10**	**9**	**8**	7	6	5	4	3	2	1
Encoded Data	**1**	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**1**

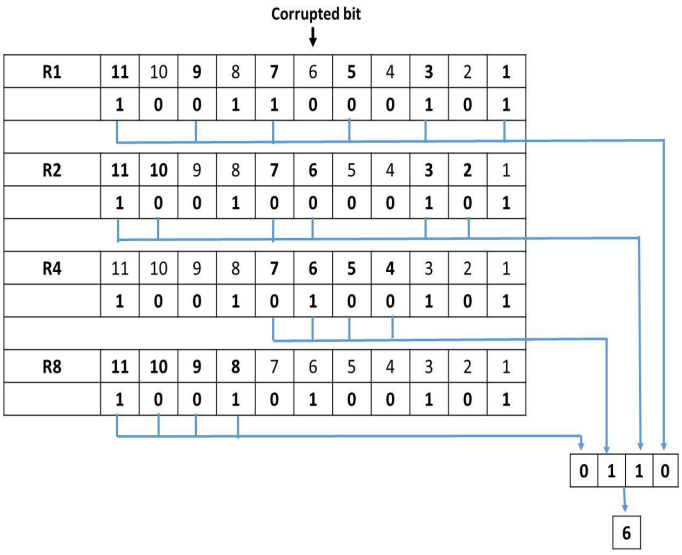

Fig 2. Hamming code error detection

B. Error detection and correction

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Suppose during the transmission, the sixth bit has changed its position from '1' to '0.' The receiver now receives the transmitted data and recalculation is done with the same bits which are sent by the sender together with the parity r bit each set has and as a result, generates four new parity bits. Then assembling of the new parity values into a binary number in a descending order of 'r' position (R8, R4, R2, and R1) is done. In the example provided, as a result of assembling, this step will result in the binary number '0110' ('6' decimal), which is the accurate location of the corrupted bit in the data packet. Once identification of bit is done, then routing error correction is done for error correction. The attractive aspect in this process is that it is easy to implement in hardware and the code correction can be done prior to receiver's knowledge.

III. SYNTHESIS

The implementation of this suggested architecture has been done in Xilinx and the synthesis output waveform with the error detection done by Hamming code is shown below.

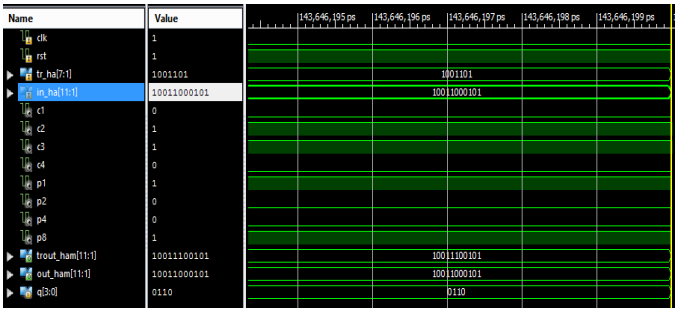

Fig 3. Synthesis result

IV. CONCLUSION

With the use of these Hamming codes, error detection becomes easier and reduces latency, thus increasing speed of packet transmission and making router reliable. So, we can precisely locate whether the data errors are located on the data bus or the input and output ports, and whether it has permanent faults or transient faults and the error correction can be done without the receiver's knowledge, thus reducing the packet transmission latency.

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