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DESIGN AND IMPLEMENTATION OF HIGH SPEED APPLICATION IN THE FIELD OF PHM ON FPGA

Vishnu kulkarni
M. Tech, Dept. of ECE, TOCE, Bangalore
vishnuk012@gmail.com

Mrs. Chrispin jiji
Asst. Prof, Dept. of ECE, TOCE, Bangalore

***Abstract*-The purpose of the paper is to develop a data acquisition system by using a Finite State machine for properly utilizing the high processing speed of the FPGA. This paper presents an FPGA-based method for high speed data acquisition and transmission taking full advantage of the parallel processing capabilities and easy to modify and upgrade features of FPGA, to cope with the difficulties of high-speed data acquisition and transmission. This paper focuses on the components, performance and characteristics of the FPGA based fault prediction and diagnosis system. FPGA as the core of data acquisition unit collects and analyses the data. This system is divided into three modules: ADC interfacing module, Artificial Intelligence Module, and Data transmission module. The ADC interfacing module, Artificial intelligence Module and Data transmission module is designed by VHDL and Spartan 3E FPGA is used for the purpose. The use of programmable FPGA hardware makes the data acquisition system design flexible, while improving the reliability of the system. It is also important for achieving the real-time online monitoring of failure.**

***Keywords*-ADC; Artificial intelligence; FPGA; high-speed data transmission**

I. INTRODUCTION

PHM seeks to use as few sensors as possible to collect data in order to evaluate the health status of a system using intelligent reasoning algorithms (such as physical model, neural network, data fusion, fuzzy logic, expert system, etc.).PHM applications can make fault forecasts before the occurrence of system fault, and provide a series of maintenance supporting measures to realize the condition based maintenance of the system with the use of all kinds of available resources. Fault diagnosis is an important prerequisite for the realization of healthy forecasts. In order to perform fault diagnosis, data acquisition and transmission are a key first step for any PHM system. So the advanced data acquisition system is the foundation for the development of PHM technology.

With extensive application of new types of Sensor, the rate of data acquisition and transmission are becoming a problem in wide variety of applications such as healthcare applications, machine health monitoring, environment and habitat monitoring, home automation, flight control system and automotive system.

Also in the scientific and technological research and industrial production, a variety of data are often needed to be collected and processed, such as weight, temperature, pressure, etc. However, a traditional data acquisition system which using a single chip or a digital signal processor (DSP) as a control device has a disadvantage of low processing speed and simple functions. Even though the use of DSP can realize a high-speed data acquisition, the cost increases as the processing speed goes up.Also, a traditional system consists of discrete devices and complex circuits. Besides, the reliability of a traditional data acquisition system is not high and it is difficult to debug the system.

A new data acquisition system based on Field Programmable Gate Array (FPGA) with its high processing speed and high reconfiguration level can solve these problems. A FPGA with its high internal clock frequency up to 100MHz, high processing speed, and programmable features, has significant advantages compared with single chip and DSP controllers. Moreover, an FPGA-based data acquisition system can process signals from different kinds of sensors such as a microphone, thermocouple and pressure transducer etc.

II. BLOCK DIAGRAM

An FPGA based intelligent data acquisition system has been proposed in this paper. The system is divided into 3 modules: ADC interfacing module, Artificial intelligence module and data transmission module.

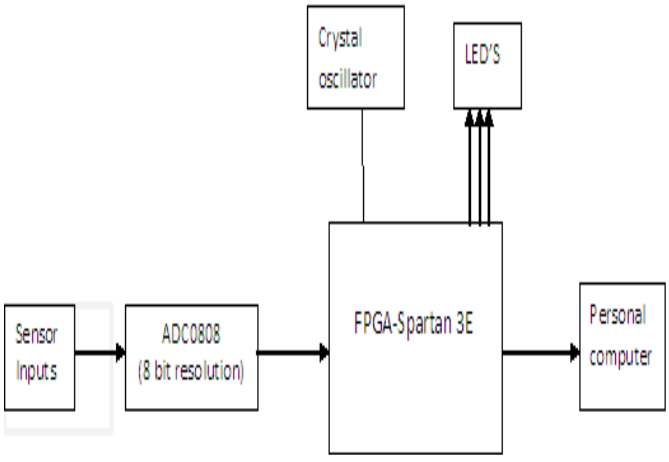

Figure 1. FPGA based Data Acquisition System

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The basic idea regarding the proposed system is that the real time data (heart beat, temperature, pressure etc) coming from the external world is sensed by the sensors and this data is of analog format. It is converted to the 8-bit digital format by using ADC0808/0809. The 8-bit data is sent to the FPGA for further analyses. This is done by ADC interfacing module. The 8-bit data is monitored continuously based on the specified conditions and accordingly control outputs are obtained. This is done by Artificial intelligence module. Data transmission module is responsible for serial transmission of data (output of ADC) from FPGA to personal computer for recording of data.

The FPGA performs the following functions:

- Managing data collection from the sensors which is carried out by using ADC module.
- Detailed analysis of collected data and making decisions based upon the threshold value (may change depending on applications) which is carried out by Artificial Intelligence module.
- Interfacing the real time data (output of ADC) to the personal computer by making use of Data transmission module.

III. ADC MODULE

ADC0808/0809 contains control logic including comparators and registers and multiplexer. There is a total of seven control signals that must be sent from the FPGA. These are the address lines, A, B, and C, Address Latch Enable (ALE), Clock, Start, and Output Enable (OE). There is also one control signal which is sent to the FPGA, it is the End of Conversion (EOC) signal.

The ADC chip has an 8 channel multiplexer there are three address select lines: A, B, and C. C is the most significant bit and A is the least. Depending on the logic levels on this address lines one of the analog channels will be selected for analog to digital conversion

.

ALE is required to load the selected address lines into the ADC. Once loaded the multiplexer sends the appropriate channel to the converter on the chip. The ALE should be pulsed for at least 100ns in order for the addresses to get loaded properly. As with all control signals it is required to have an input value of Vcc - 1.5 up to 15V for a high and 1.5V down to -0.3V for a low. The following control signals are used to control the conversion.

The clock signal is required to cycle through the comparator stages to do the conversion. There are 8, 8 clock cycle periods required in order to complete an entire conversion. This means that an entire conversion takes at least 64 clock cycles. (Up to 72 if the start signal is received in the middle of an 8 clock cycle period.) .The maximum frequency of the clock is 1.2MHz. The maximum clock frequency is affected by the source impedance of the analog inputs. It is recommended that the source resistance not exceed 5kohms for operation at 1.2MHz and 10komhs for operation at 640 kHz. When operating ADC at 500 kHz and below the ALE signal and the start signal is tied together. This is how the ADC is designed in VHDL code used.

The purpose of the start signal is two fold. On the rising edge of the pulse the internal registers are cleared and on the falling edge of the pulse the conversion is initiated. Like the ALE pulse the minimum pulse width is 100ns. The signal can be tie to the ALE signal when the clock frequency is below 500 kHz.

The Output Enable signal causes the ADC to actually output the digital values on the output lines. The ADC stores the data in a tri-state output latch until the next conversion is started, but the data is only output when enabled. In this implementation the OE signal is pulsed high one clock cycle after the EOC signal goes high and remains high until the data is safely stored into the desired register in the FPGA.

The End of Conversion signal is sent to the FPGA from the ADC. The signal goes low once a conversion is initiated by the start signal and remains low until a conversion is complete.

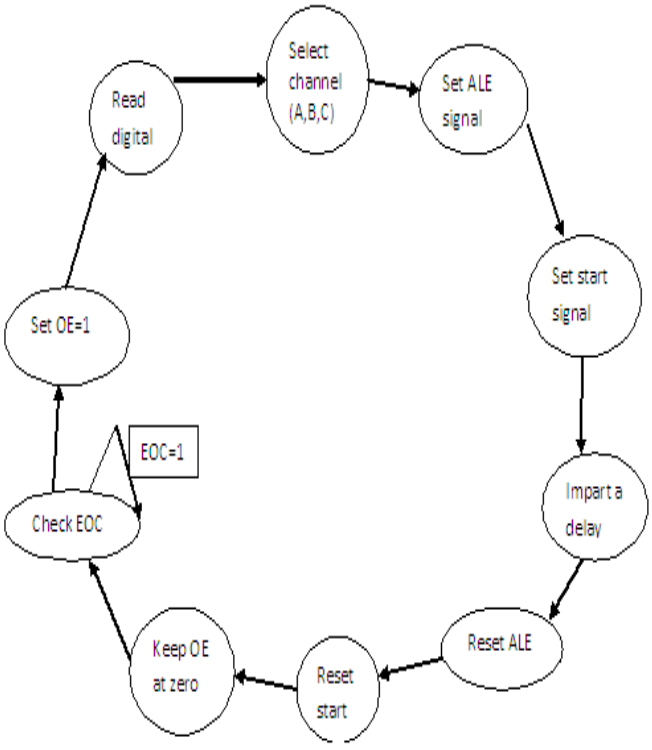

Figure 2. Sequence Diagram of ADC interfacing

Based on the above state machine the ADC module is designed by using VHDL.

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IV. ARTIFICIAL INTELLIGENCE MODULE

The Core module (heart of the project) for processing the 8-bit data i.e. condition based data monitoring in real time is done using artificial intelligence module.
Data processing involves monitoring of data in detailed manner with 3 conditions (may change depending on requirements):

1. Specific Threshold value: The 8 bit data is compared with the threshold value (may change depending on requirements) and a decision is made accordingly.
2. Rate of change: The difference between two values (1st sensed and 2nd sensed data) is compared with another threshold value (may change depending on requirements) and accordingly decision is made.
3. Specific interval of time: The data after specific time interval is compared with another threshold value (may change depending on requirements) and decision is made.

V. DATA TRANSMISSION MODULE

Uart is used as external communication interface wherein it is used as data transmission module the the 8-bit data (from the output of ADC) from FPGA to Personal computer serially. A universal asynchronous receiver/transmitter (UART) receives serial data and stores it as parallel data, usually one byte. It also takes parallel data and transmits it as serial data. Such serial communication is beneficial when we need to communicate bytes of data between devices that are separated by distances or when those devices simply have few available I/O pins.

Internally a simple UART may possess some configuration registers, and two independently operating processors, one for receiving and the other for transmitting. The transmitter may possess a register, often called a transmit buffer, that holds data to be sent. This register is a shift register, so the data can be transmitted one bit at a time by shifting at the appropriate rate. Likewise the receiver receives data into a shift register and then this data can be read in parallel.

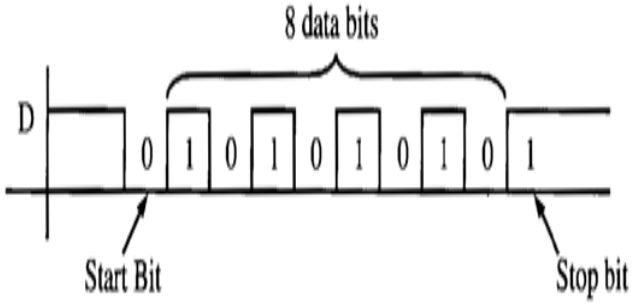

figure 3: standard serial data format

The figure 3 shows standard format for serial data transmission. Since there is no clock line, the data (D) is transmitted asynchronously, one byte at a time. When no data is being transmitted, D remains high. To mark the start of the transmission, D goes low for one bit time, which is referred to as the start bit. Then 8 data bits are transmitted, least significant bit (LSB) first. After 8 bits are transmitted D must go high for at least one bit time, which is referred to as the stop bit. Then transmission of another byte can start at any time. The number of bits transmitted per second is frequently referred to as the BAUD rate.

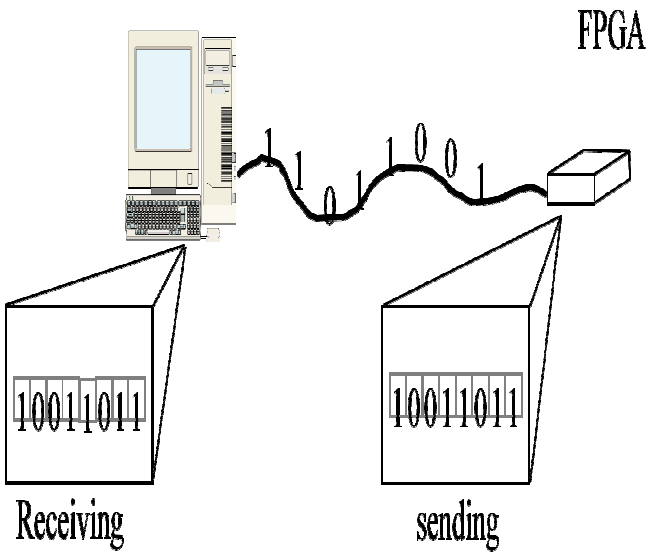

figure 4: Transmission of Real time Data from FPGA to PC

The transmission with 8 data bits, no parity, and 1 stop bit. Note that the LSB of the data word is transmitted first. No clock information is conveyed through the serial line. Before the transmission starts ,the transmitter and receiver must agree on a set of parameters in advance, which include the baud rate (i.e., number of bits per second), the number of data bits and stop bits, and use of the parity bit. The commonly used baud rates are 2400, 4800, 9600, and 19,200 bauds. The UART protocol is designed by using VHDL and the baud rate set as 9600bps.

VI. RESULT DISPLAY

The Proposed system consists of three modules: ADC interfacing module, Artificial intelligence module and data transmission module.
These three modules are designed by VHDL and synthesized by using Xilinx ISE 12.2 version tool. The functionality of the design is verified by simulating the code by using the Modelsim tool and the waveforms are obtained.

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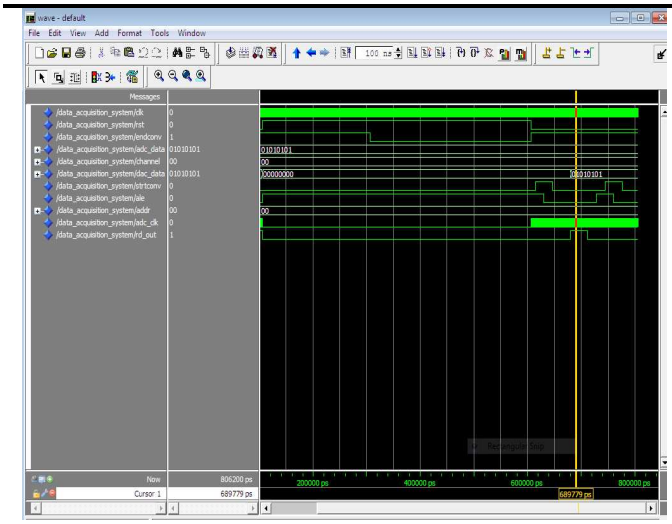

Figure 5. simulation waveforms of ADC module

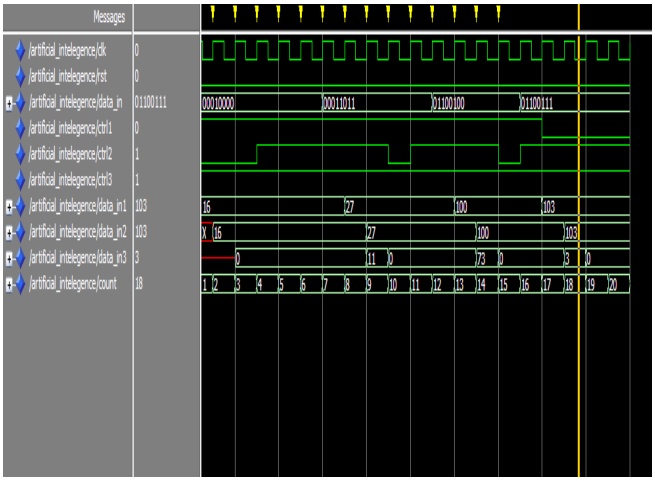

Figure 6. simulation waveforms of Artificial intelligence module

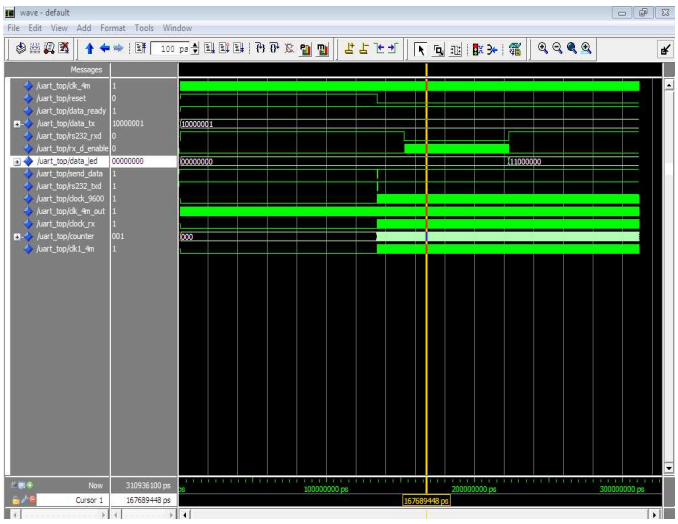

Figure 7. simulation waveform of Data transmission module

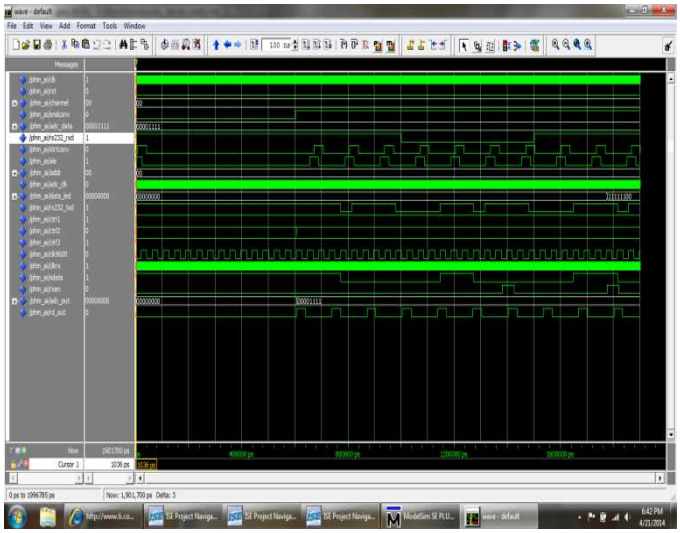

Figure 8. simulation waveforms of the entire top module(integration of ADC module, artificial intelligence module and Data transmission module)

VII. CONCLUSION AND FUTURE SCOPE

The ever increasing cost associated with developing an ASIC and the long development cycles do not work for many of the applications. These applications are better served by using FPGA based platforms. Hence this paper comes to conclude that Spartan 3E FPGA interface provide a flexible and versatile platform for building high speed data acquisition to all the latest ADC devices available on the market. The system proposed also has the advantage of collecting data from different sensors.

This paper also concludes that it makes use of the programmable characteristic of the FPGA hardware to make the software and hardware design of the whole data acquisition system flexible and improve the reliability of system. Therefore, it is of great significance to real time monitoring of data.

When we see the height of flexibility we are getting, future assures to be very promising and advantageous. We get the confidence that we can build anything using this technology.

ACKNOWLEDGEMENT

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