Enhancement of Low Power Pulse Triggered Flip-Flop Design Based on Signal Feed-Through Scheme using Pulse-Enhance

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Abstract: **Low Power research major concern in today's VLSI word. Practically, clocking system like flip-flop (FF) consumes large portion of total chip power. So in this paper we discuss about the design of the clock system using novel Flip-Flop design. In this paper, a novel low-power pulse-triggered flip-flop (FF) design is presented. Pulse- triggered FF (P-FF) has been considered as a popular alternative to the conventional master – slave based F. a low-power flip-flop (FF) design featuring an explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through scheme is presented. The proposed design successfully solves the long discharging path problem in conventional explicit type pulse-triggered FF (P-FF) designs and achieves better speed and power performance in the applications of high speed. These circuits are simulated using Tanner Tools with TSMC018 technology**.

Keywords: **pulse-triggered flip-flop (FF), true single phase clock latch, clocking system**

1. INTRODUCTION

Flip-flops (FFs) are the basic storage elements and they are used extensively in designs of all digital system. Today's technology adopts the pipelined architecture n each and every system to improve its performance. Clock system consists of a clock generator, clock distribution network and no of Flip-Flops. It is also estimated that the power consumption of the clock system, is as high as 30% to 60% of the total system power. In order to reduce the CDN load and to reduce the clock power we introduce a pulse triggered flip flops. Pulse-triggered FF (P-FF) has been considered a major alternative to the conventional master–slave-based FF in the applications of high-speed operations [7]–[4]. Along with the speed advantage, its circuit simplicity is also used to lowering the power Consumption of the clock tree system. Instead of traditional Master-Slave Flip-Flop a P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master–slave configuration, is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. P-FFs are thus less sensitive to clock jitter. Despite these advantages, pulse generation circuitry requires delicate pulse width control in the face of process variation and the configuration of pulse clock distribution network .Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit [9]. In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power economical than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Implicit-type designs have lengthened discharging path in latch design, which leads to inferior timing characteristics. The situation deteriorates further when low-power techniques such as conditional capture, conditional pre-charge, conditional discharge, or conditional data mapping are applied. As a consequence, the transistors of pulse generation logic are often enlarged to assure that the generated pulses are sufficiently wide to trigger the data capturing of the latch. Explicit-type P-FF designs face a similar pulse width control issue, but the problem is further complicated in the presence of a large capacitive load, e.g., when one pulse generator is shared among several latches. In this paper, we will present a novel low-power explicit-type P-FF design featuring a conditional pulse-enhancement scheme. Three additional transistors are employed to support this feature. In spite of a slight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced. This gives rise to competitive power and power–delay–product performances against other P-FF designs.

2. EXPLICIT PULSE TRIGGERED FLIP-FLOP:

Explicit Pulse triggered Flip-Flop consists of Pulse generator and a Latch network
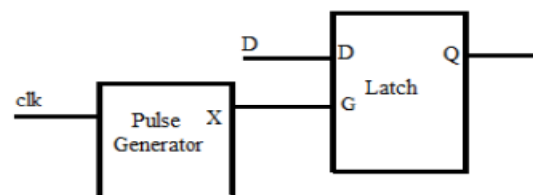
Fig(a): Block Diagram of Pulse Triggered Flip-Flop

Where as in Pulse triggered flip flops, a short pulse around the rising (or falling) edge of the clock is created through a pulse generator circuit. This pulse acts as the clock input to a latch. Sampling of latch is done in this short window created by the pulse generator

Pulse Generator: The Pulse generator consists of and gate and whose inputs are clk and another was delayed of clock signal by three inverters which will be used for generating the strobe signals. Latch network was designed by the basic True Single Phase Latch (TSPC) latch. The basic Explicit Flip-Flip was Ex-Dco(Explicit Data Close Flip-Flop)Flip-Flop as shown below.

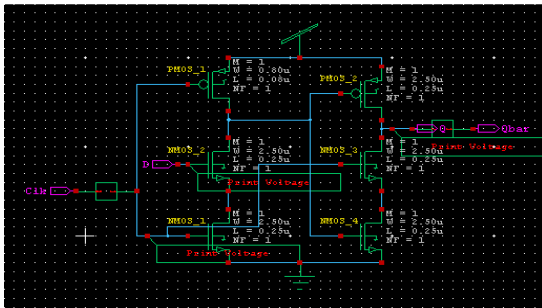
Fig1: Explicit Data Close Flip-Flop

In Explicit Data Close Flip-Flop it has a unwanted discharge problem whenever it has static input 1 case. In order to reduce we introduce a Conditional discharge mechanism to reduce power dissipation.
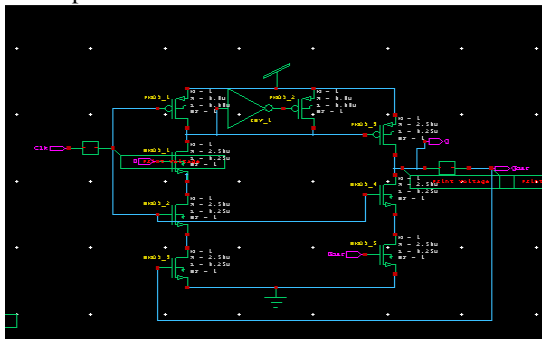

Fig2: CDFF Flip-Flop

An extra nMOS transistor controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1." In addition, the keeper logic for the internal node X is simplified and consists of an inverter plus a pull-up pMOS transistor. The schematic diagram of the proposed flip-flop, conditional discharge flip-flop (CDFF), is shown above. It uses a pulse generator as in [9], which is suitable for double-edge sampling. The flip-flop is made up of two stages. Stage one is responsible for capturing the LOW-to-HIGH transition. If the input is HIGH in the sampling window, the internal node is discharged, assuming that were initially (LOW, HIGH) for the discharge path to be enabled. As a result, the output node will be charged to HIGH through PMOS of D input in the second stage. Stage 2 captures the HIGH-to-LOW input transition. If the input was LOW during the sampling

period, then the first stage is disabled, and node retains its pre-charge state. Whereas, node will be HIGH, and the discharge path in the second stage will be enabled in the sampling period, allowing the output node to discharge and to correctly capture the input data Static CDFF has same operation but it doesn't consist of pre-charging as present in dynamic structure. So, its take longer time for processing.
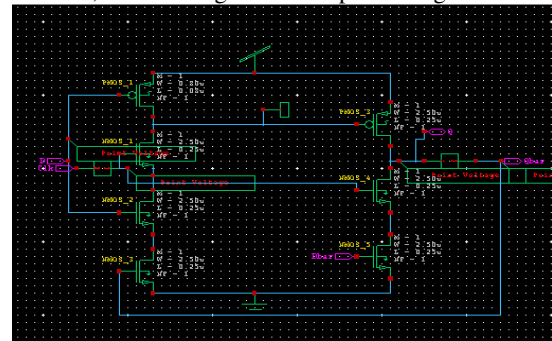

Fig3: Static CDFF structure

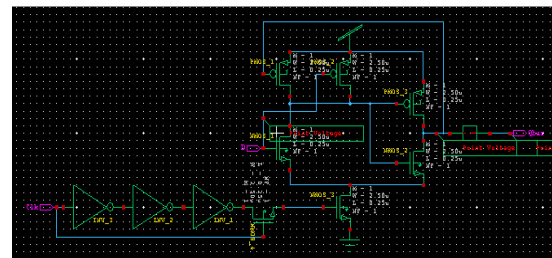**Modified Hybrid Latch Flip-Flop:**

Fig 4: MHLFF

In MHLFF we reduce the longer stack of NMOS transistor at output node in order to increase the speed of the Flip-Flop. It also flows the static latch structure whose pre-charging was depend on the data. MHLFF drawback is that internal node becomes floating when output Q and input Data both equal to "1". Extra DC power emerges if node X is drifted from an intact "1".
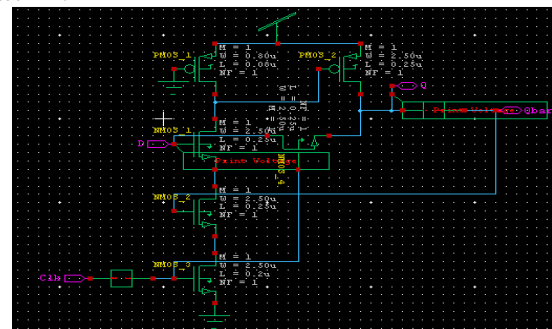

Fig5: Proposed Flip-Flop

They there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style

design, and the charge keeper circuit for the internal node *X* can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node *X*. Second, a pass transistor controlled by the pulse clock is included so that input data can drive node Q of the latch directly. The pull down network of output node was reduced so the we reduce the discharge path.
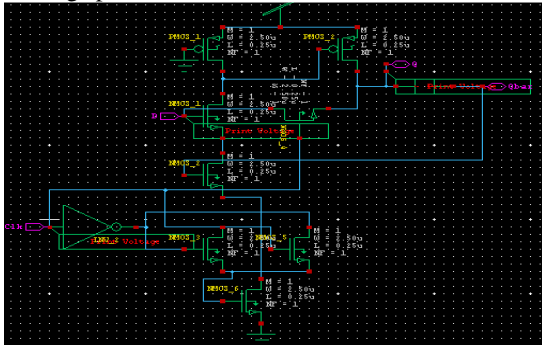

Fig6: Proposed Flip-Flop with Enhance Pulse

The proposed Flip-Flop consists of 24 transistors are used to design the Flip-Flop. In order to reduce the no of transistor count here we introduce Pass transistor based pulse generator design which useful to reduce the no of transistors so as the power dissipation.

3. SIMULATION

These Flip-Flops are designed and simulated using T-Spice using TSMC018 Technology.

Circuit	Power dissipation
Ep DCO	1.9001885e-005watts
CDFF	2.4174760e-005watts
SCDFF	3.4992420e-005watts
MHLFF	2.3020230e-005watts
PROPOSED FLIPFLOP	1.616579e-005watts
PROPOSED FF WITH PULSE ENHANCE	1.048501e-005watts

4. CONCLUSION

In this brief, we presented a P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of a pass transistor and pseudo-nMOS logic and it consist of Pulse generator design. The main idea was to provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The was made the existing flip flop can be designed using less no of transistor count as well as power dissipation.

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