International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 5, Issue 11, November 2018)

Modeling and Simulation of 9-Level Inverter

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Abstract: - **The paper shows a plan that is utilized to improve the limit of the PV cell alongside independent battery used to encourage the acceptance engine drive. The power limit is expanded by utilizing 9-level inverter and it is practically equivalent for the instances of Neutral Point Clamped Multi level inverter and Cascade – H – Bridge inverter. Since the power level stays same for the previously mentioned topologies, here fundamental concentrate is on the THD content for the distinctive topologies.**

Keywords: **Energy Management, Induction Motor, Multi Level Inverter, Multi Level SPWM, PV Battery, and THD**

1. INTRODUCTION

Solar power is the abundantly available source which has no noise and pollution during its production compared with conventional energy sources hence the solar power is the upcoming source of energy for future needs. Solar Energy is trapped and converted in to electricity with the help of PV cells. PV cells are more useful for remote areas where conventional energy sources are not reachable. Rapid evolution in semiconductor devices has revolutionised the industry for increasing in the production of high power applications. The above mentioned reasons lead to the development of multilevel inverter. Difficulties of commutation failure, harmonics and total input voltage problems are minimized as the level of inverter is increased. Different Control Algorithms are used by the multi level inverter [2-4] of which Sinusoidal Pulse Width Modulation (SPWM) appears most suitable. In multi level inverter as the level increases the THD decreases, also the output signals will have good spectral quality. Multi level inverters are mostly suited for high power applications [3-6].Disadvantage of multi level inverter design of control circuit is much complex and due to which it is not widely used for industrial applications [7-8].

2. PHOTOVOLTAIC SYSTEM

Photovoltaic cell characteristics are strongly nonlinear and the pv cell performance is characterised by:

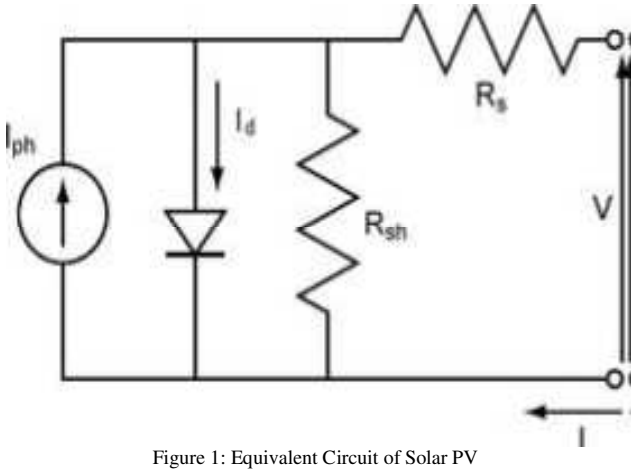

Figure 1: Equivalent Circuit of Solar PV

As shown in the figure-1, IPh is the short circuit current of PV cell and RS is the series resistance, RSh is the shunt resistance, Id is the diode current. The operation of PV cell is characterized by the fallowing equation

$$I=I_{Ph}-I_0[e^{\frac{q(V+IR_S}{AKT}}-1]-\frac{V+IR_S}{R_{Sh}}$$

Where,
IPh= Photo-generated current (A)
I= Cell output current (A)
I0=Diode Saturation Current (A)
V=Cell Output Voltage (V)
Rs=Series Resistor (Ω)
e= Electron Charge 1.6×10-19 (coul)
K=Boltzmann Constant (j/K)
T=cell temperature
Due to the robustness and the satisfactory performance of the three phase induction motor it is widely used in various kinds of industrial applications. Whatever the research work done main focus was on the development of Control Algorithm. Cost, Simplicity and flexibility of the drive was not given much importance. This paper gives a new approach so that the cost and flexibility of the drive are taken into picture during the design process of the induction motor drive.

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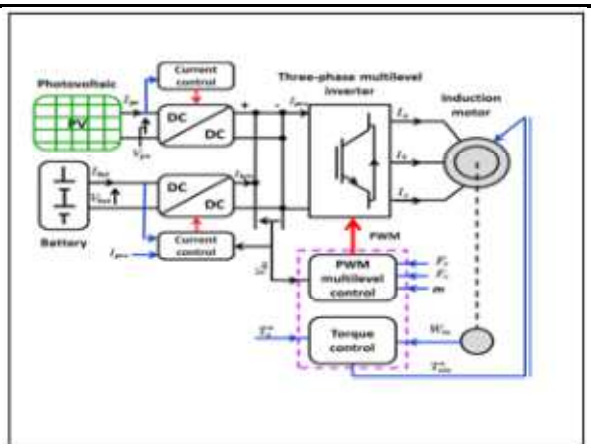

Figure 2: Induction Motor Driven by PV-Batteries Standalone System Using a Controlled Multilevel Inverter

3. MULTILEVEL INVERTER CONTROL STRATEGIES

The Three-Level Inverter Control Strategy

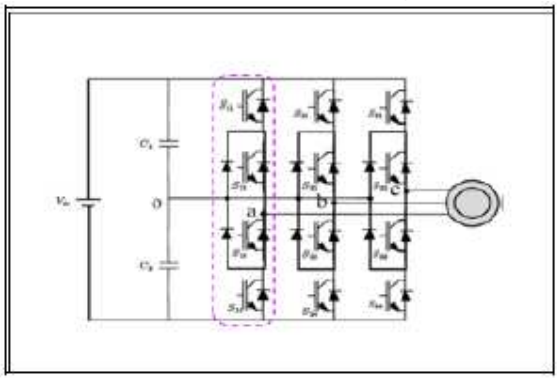

Figure 3: Three-Level Three Phase Inverter

Figure (3) shows a three phase three level inverter.V**ao** is the phase voltage between phase a and neutral 'o'.The three level NPC inverter is used [10] for medium voltage, high power application.

Table 1

Sequence	Switches State		Output Phase (v_{ao}) Voltage
	ON	OFF	
1	S_{11},S_{12}	S_{13}, S_{14}	$+v_{dc}/2$
2	S_{12},S_{13}	S_{11}, S_{14}	0
3	S_{13}, S_{14}	S_{11},S_{12}	$-v_{dc}/2$

These '3' sequences are applied periodically.9 level NPC multi level technique is used. In SPWM technique the modulating wave is compared with reference waves both in the +ve and –ve halves. The comparator output is sent to the switches to generate phase output voltages.

CASCADED H-BRIDGE INVERTER

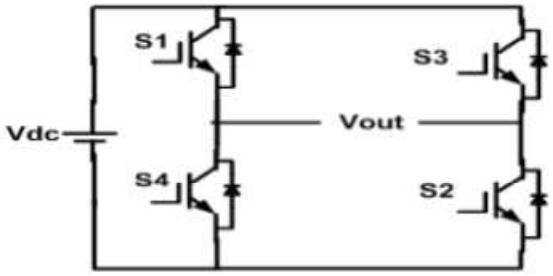

Figure 4: Circuit of the Single Cascaded H-Bridge Inverter

For the above single phase three level inverter the switch positions and the output voltages are as fallows.

Table 2

Switches		Voltage Level
ON State	OFF State	
S1,S2	S3,S4	+Vdc
S3,S4	S1,S2	-Vdc
S4,D2	S3,D1	0

In the cascaded H-bridge inverter
Output voltage level=2x+1
Voltage step of each level=Vdc/(2x)
Where x=no of cascaded H-bridges
The selection scheme of 5 level CHB and the output voltages are as follows:

Table 3

Switches at ON Stage	Diodes at ON Stage	Voltage Level
S1,S2	-	+Vdc
S1,S2,S5,S6	-	+2 Vdc
S4,S8	D2,D6	0
S3,S4	-	-Vdc
S3,S4,S7,S1	-	-2 Vdc

The available PWM techniques for CHB inverter are
- Phase Shifted PWM (PSCPWM)
- Level shifted PWM (LSCPWM)

Phase Shifted PWM (PSCPWM)

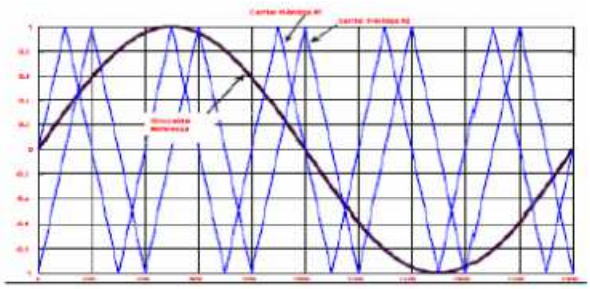

Figure 5: Phase Shifted Carrier PWM

For Y voltage levels (Y-1) carrier signal required and they are phase shifted with an angle θ=(360°/Y-1).The gate signals are

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generated with proper comparison of carrier wave and modulating signal.

Level Shifted PWM (LSCPWM

For carriers signals, the time values of each carrier waves are set to [0 1/600 1/300] while the outputs values are set according to the disposition of carrier waves. After comparing, the output signals of comparator are transmitted to the IGBT This technique is divided into 3 types

- **In Phase Disposition**

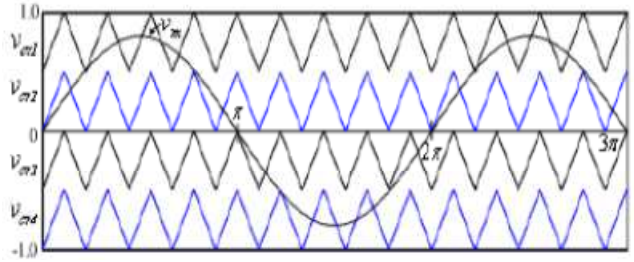

Figure 6: Level Shifted Carrier PWM (IPD)

All carrier signals are in phase.

- **Alternative Phase Opposition**

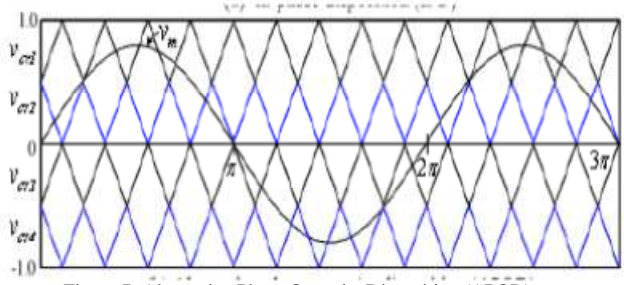

Figure 7: Alternative Phase Opposite Disposition (APOD)

All carrier signals are alternatively phase opposite disposition.

- **Phase Opposite Disposition**

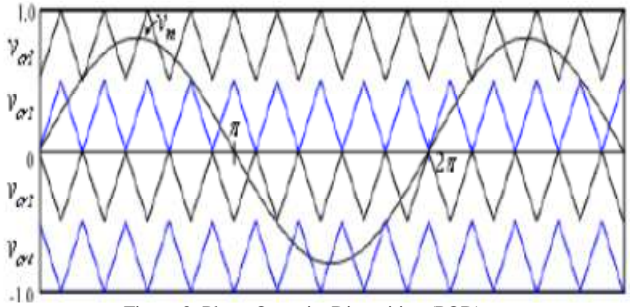

Figure 8: Phase Opposite Disposition (POD)

All carriers above zero reference are phase but in opposition with those below the zero references. Among the above 3 cases, IPD give better harmonic performance.

4. MATLAB MODELING AND SIMULATION RESULTS

Here simulation is carried out in two different configurations,
1). Implementation of Proposed Concept using Neutral Clamped Type Multilevel Inverter.
2).Implementation of Proposed Concept using Cascaded H-Bridge Multilevel Type Inverter.

Case 1: Implementation of Proposed Concept using Neutral Clamped Type Multilevel Inverter.

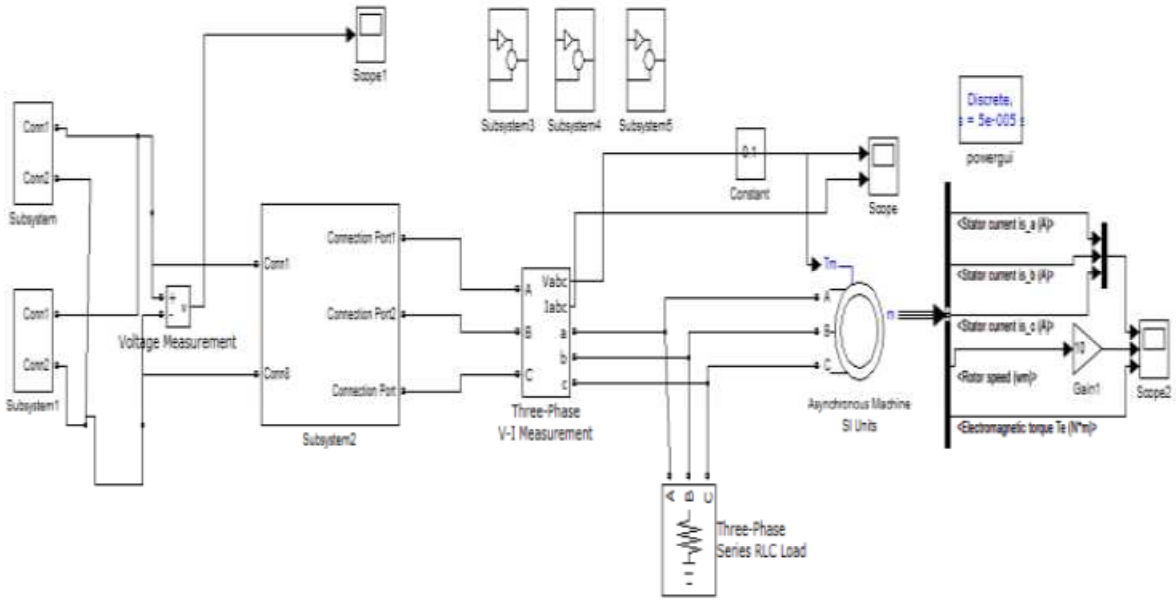

Figure 9: Matlab/ Simulink Model of Proposed NPC Converter with Induction Machine Drive

Figure 9 shows the Matlab/Simulink Model of Proposed NPC Converter with Induction Machine Drive.

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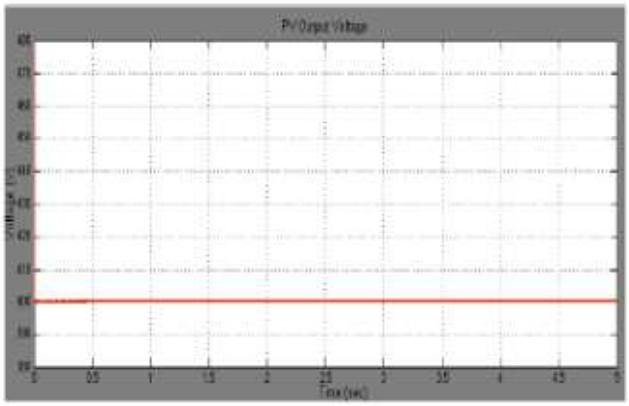

Figure 10: PV Output Voltage

Figure 10 Output Voltage coming from PV arrays with the help of high step up DC/DC Converter and directly fed to our proposed inverter.

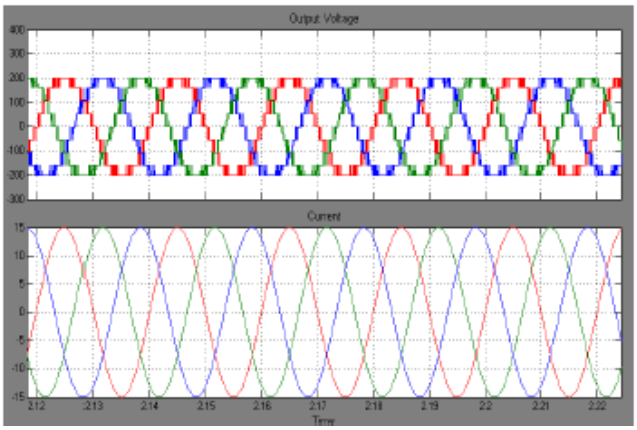

Figure 11: Level Output Voltage and Current

Figure 11 shows the 9-Level Output Voltage and current coming from the proposed NPC multilevel inverter.

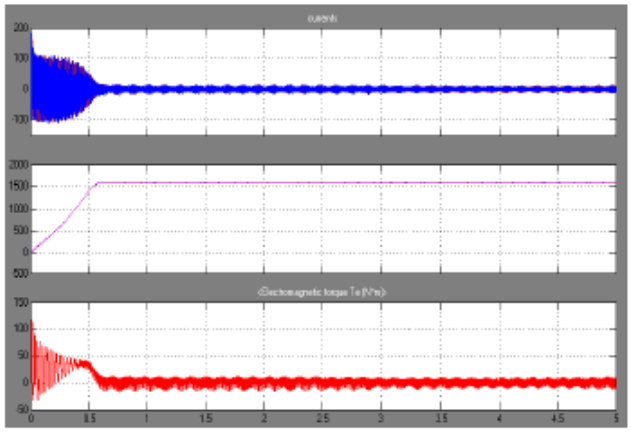

Figure 12: Stator Currents, Speed, Electromagnetic Torque

Figure 12 shows the Stator Currents, Speed, and Electromagnetic Torque of the proposed NPC Strategy Controlled Drive Performance Characteristics.

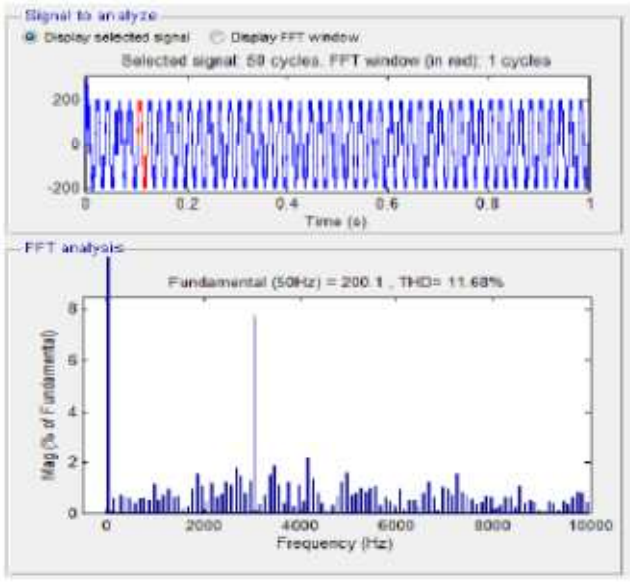

Figure 13: FFT Analysis of Proposed NPC Converter Output Voltage

Figure 13 shows the FFT Analysis of Proposed NPC Converter Output Voltage, we get 15.18% no need of any filter we get this value.

Case 2: Implementation of Proposed Concept using Cascaded H-Bridge Multilevel Type Inverter

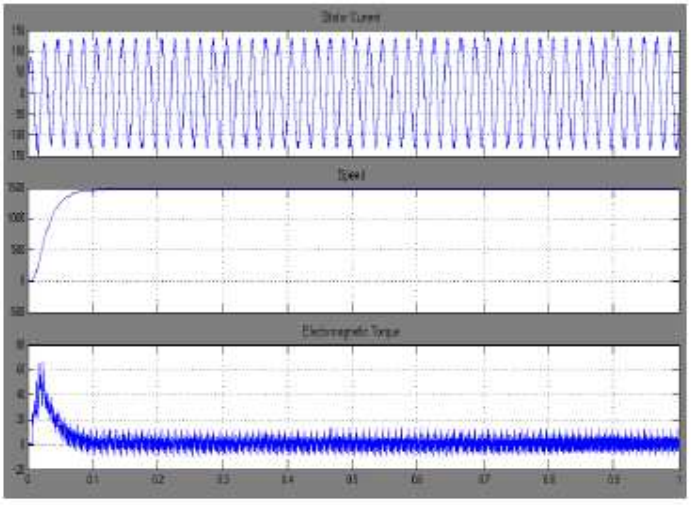

Figure 14: Stator Currents, Speed, Electromagnetic Torque

Figure 14 shows the Stator Currents, Speed, and Electromagnetic Torque of the proposed CHB Multilevel Inverter to Controlled Drive Performance Characteristics.

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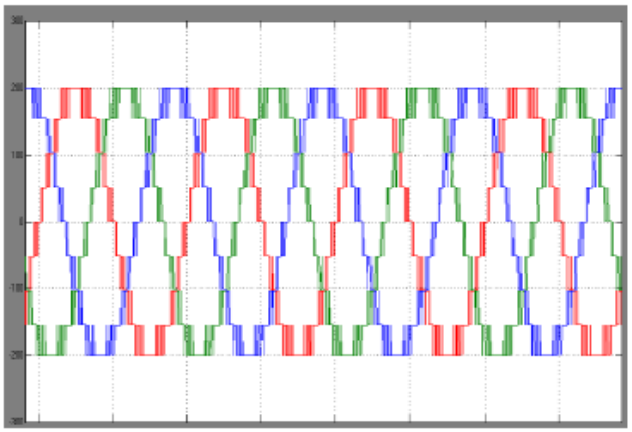

Figure 15: 9- Level Output Voltage

Figure 15 shows the 9-Level Output Voltage and coming from the proposed CHB Multilevel Inverter.

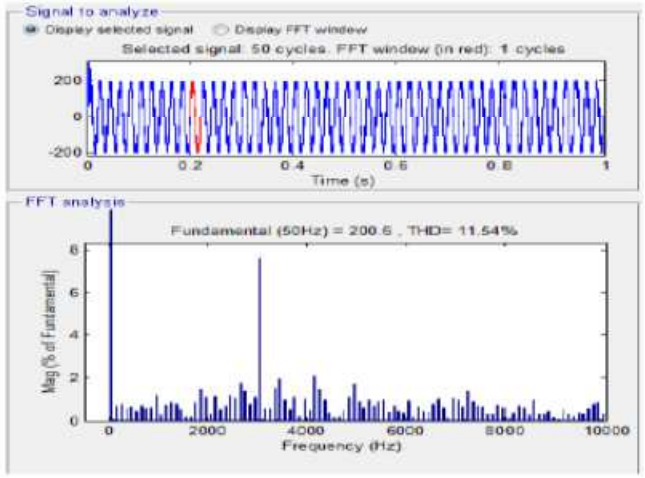

Figure 16: FFT Analysis of Proposed CHB Multilevel Converter Output Voltage

Figure 16 shows the FFT Analysis of Proposed CHB Multilevel Converter Output Voltage, we get 15.18% no need of any filter we get this value.

5. CONCLUSIONS

In this paper, a general multilevel SPWM control calculation for 9-level inverter has been demonstrated and mimicked utilizing Matlab®/Simulink with various topologies. This calculation can produce consequently SPWM beats for any level of inverter by changing just a parameter n which is the quantity of inverter level. Reproduction of nine inverter of NPC topology and CHB Multilevel Converter is associated with acceptance engine has been performed and the created signals THD is examined. The framework is provided by a PV board and batteries bank. That gives vitality independence to the framework. Reenactment comes about give a superior nature of stator current as far as low sounds, in this manner lessening the antagonistic consequences for of the machine life and in the long run the electrical system which supplies it, and decreases the switch tally, low exchanging misfortunes, and so on.

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