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Design and Verification of Non-Integer Clock Divider to Improve Performance

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Abstract:- **The divider is the one of the most important module in micro-processors. A new algorithm was proposed to realize the decimal frequency divider with any number divided ratio, and the ratio was configurable divide by the I2C.In statistical periods, the divide ratio is adjusted dynamically by calculating the error of clock. Error of divider can be minimized after few rounds. The experimental result indicated that the decimal frequency divider takes fewer resources. Inter-Integrated Circuit, I2C is a serial bus short distance protocol developed by Philips Semiconductor. I2C is appropriate for interfacing to devices on a single board, and can be stretched across multiple boards inside a closed system.**

Keywords: **I2c, Loop, PLL, Clock, Frequency, divider**

1. INTRODUCTION

1.1 PHASE LOCKED LOOP

A phase-locked loop or phase lock loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. While there are several differing types, it is easy to initially visualize as an electronic circuit consisting of a variable frequency oscillator and a phase detector. The oscillator generates a periodic signal. The phase detector compares the phase of that signal with the phase of the input periodic signal and adjusts the oscillator to keep the phases matched. Bringing the output signal back toward the input signal for comparison is called a feedback loop since the output is 'fed back' toward the input forming a loop.

Keeping the input and output phase in lock step also implies keeping the input and output frequencies the same. Consequently, in addition to synchronizing signals, a phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency. These properties are used for computer clock synchronization, demodulation, and frequency synthesis.

Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to demodulate a signal, recover a signal from a noisy communication channel, generate a stable frequency at multiples of an input frequency (frequency synthesis), or distribute precisely timed clock pulses in digital logic circuits such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a hertz up to many gigahertz.

CLOCK GENERATION

Many electronic systems include processors of various sorts that operate at hundreds of megahertz. Typically, the clocks supplied to these processors come from clock generator PLLs, which multiply a lower-frequency reference clock (usually 50 or 100 MHz) up to the operating frequency of the processor. The multiplication factor can be quite large in cases where the operating frequency is multiple gigahertz and the reference crystal is just tens or hundreds of megahertz.

CLOCK DISTRIBUTION

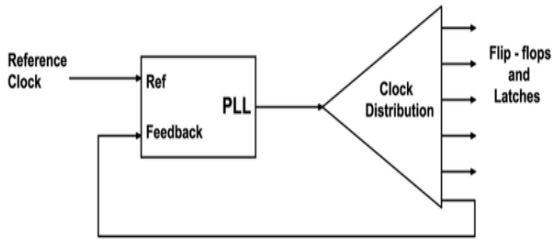
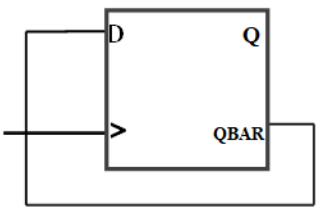


Fig1. Clock distribution

Typically, the reference clock enters the chip and drives a phase locked loop (PLL), which then drives the system's clock distribution. The clock distribution is usually balanced so that the clock arrives at every endpoint simultaneously. One of those endpoints is the PLL's feedback input. The function of the PLL is to compare the distributed clock to the incoming reference clock, and vary the phase and frequency of its output until the reference and feedback clocks are phase and frequency matched.

1.2 Frequency Divider

A frequency divider is a circuit that takes an input signal of a frequency fin and generates an output signal of a frequency fout fout=fin/n n is an integer. A frequency divider is used in a frequency synthesizer which is used to generate a new frequency from a single stable reference frequency.



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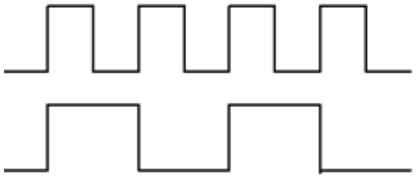

Fig:1.1 Frequency Divider

1.2.1 Types of Frequency Divider

Frequency dividers are divided into:

1) Analog Divider
2) Digital Divider

Analog Divider:

Analog frequency dividers are used only at very high frequencies.

Regenerative frequency divider:

A regenerative frequency divider mixes the input signal with the feedback signal from the mixer.

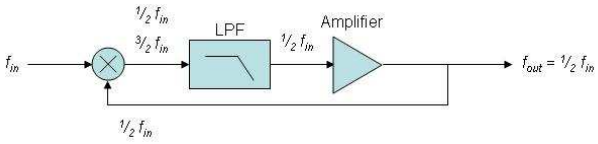

Fig:1.2 Regenerative frequency divider

The feedback signal is $f_{in}/2$. This produces sum and difference frequencies $f_{in}/2$, $3f_{in}/2$ at the output of the mixer. A low pass filter removes the higher frequency and the $f_{in}/2$ frequency is amplified and fed back into mixer.

Digital Divider:

Digital dividers implemented in modern IC technologies can work up to tens of GHz. A simple binary counter can be used, clocked by the input signal. The least-significant output bit alternates at 1/2 the rate of the input clock, the next bit at 1/4 the rate, the third bit at 1/8 the rate, etc

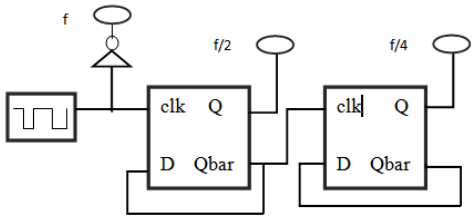

Fig:1.3 Digital Divider

An arrangement of flip-flops are a classic method for integer-n division. Such division is frequency and phase coherent to the source over environmental variations including temperature. The easiest configuration is a series where each flip-flop is a divide-by-2. For a series of three of these, such system would be a divide-by-8. By adding additional logic gates to the chain of flip flops, other division ratios can be obtained. Integrated circuit logic families can provide a single chip solution for some common division ratios.

Another popular circuit to divide a digital signal by an even integer multiple is a Johnson counter . This is a type of shift register network that is clocked by the input signal. The last register's complemented output is fed back to the first register's input. The output signal is derived from one or more of the register outputs. For example, a divide-by-6 divider can be constructed with a 3-register Johnson counter. The three valid values for each register are 000, 100, 110, 111, 011, and 001. This pattern repeats each time the network is clocked by the input signal. The output of each register is a f/6 square wave with 60° of phase shift between registers. Additional registers can be added to provide additional integer divisors.By using digital dividers we can divide the frequencies according to the user requirement, which can reduce the number of crystals in the design and it will reduce the cost of design and also printed circuit board size.

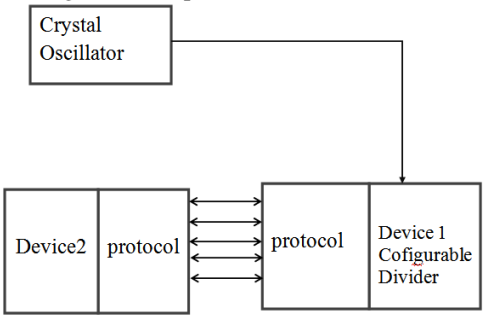

Fig 1.4 Block diagram of frequency divider

Crystal Oscillator:

An oscillator that produces electrical oscillations at a frequency determined by the physical characteristics of a piezoelectric quartz crystal Oscillators are an important component of radio frequency (RF) and digital devices. Today, product design engineers often do not find themselves designing oscillators because the oscillator circuitry is provided on the device. However, the circuitry is not complete. Selection of the crystal and external capacitors have been left to the product design engineer. If the incorrect crystal and external capacitors are selected, it can lead to a product that does not operate properly, fails prematurely, or will not operate over the intended temperature range. For product success it is important that the designer understand how an oscillator operates in order to select the correct crystal.

Selection of a crystal appears deceivingly simple. Take for example the case of a microcontroller. The first step is to determine the frequency of operation which is typically one of several standard values that can be selected from a catalog, distributor, or crystal manufacturer. The second step is to sample or purchase the crystal and evaluate it in the product design.

Configurable Divider:

If the crystal oscillator frequency is 40MHz, but the required frequency is 220.805, so we need to divide the

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frequencies into 181.55, so divider adjust frequency of the clock using the clock error which is calculated by changing clock period dynamically.
Configurable divider divides any frequencies according to user requirement

1.3 Protocols:

1.3.1Serial Peripheral Interface:- The Serial Peripheral Interface or SPI bus is a synchronous serial data link standard named by Motorola that operates in full duplex mode.
-A clock signal named SClk,sent from bus master to all slaves,all the SPI signals are synchronous to this clock signal.
-A Data line from the master to the slaves, named MOSI (Master Out_Slave In).
-A Data line from the slave to the master, named MISO(Master In-Slave Out).

1.3.2 Inter-integrated Circuit (I2C/IIC):

I2C is a Multi-Master serial single ended computer bus invented by Philips used for attaching low-speed peripherals to a mother-board,embeded system,cellphone or other devices.
I2C is a two wire serial interface:
1)Serial Data Line (SDA-bidirectional)
2)Serial Clock Line (SCL)

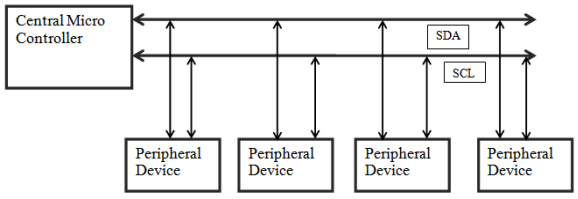

Fig 1.6 Block diagram of Inter-Integrated Circuit protocol

All I2C bus compitable devices incorporate an on-chip interface which allows them to communicate directly with each other via the I2C bus.This design concept solves the many interfacing problems encountered when designing digital control circuits.

Designer Benfits:

- Functional blocks on the block diagram correspond with actual ICs, design proceed rapidly from block diagram to final schematic.
- No need to design bus interface because the I2C bus interface is already integrated on-chip
- Integrated addressing and data-transfer protocol allow systems to be completely software defined.
- The same IC types can often be used in many different applications.
- Design-time reduces as designers quickly become familiar with the frequently used functional blocks represented by I2C bus compatible I2Cs.
- ICs can be added or removed from a system without any other system.
- Fault diagnosis and debugging are simple, malfunctions can be immediately traced.
- Low current consumption
- High noise immunity.
- Software development time can be reduced by assembling a library of reusable software modules.

I2C available in:

General purpose circuits like LCD drivers, remote input, output ports, RAM, EEPROM or data converters.
Some intelligent control, usually a single chip microcontroller.
Application-oriented circuits such as digital tuning and signal processing circuits for radio and video systems or DTMF generators for telephones with tone dialing.

Algorithm:

1.4 Decimal frequency Divider:

If K is the dividing ratio of decimal frequency divider, then K can be expressed as K=N+A/B, N is the integer part of K, and the part of decimal part can always be expressed as A/B. There are many methods to realize decimal frequency divider, but the basic theory is calculating one more or one less pulse in several periods to get a value of decimal frequency divider in the periods by statistical and average sense.

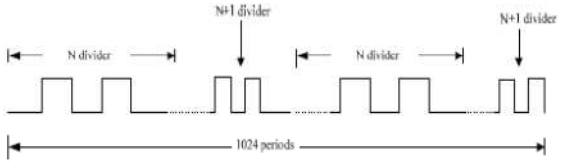

Fig 1.7 Block diagram of divider circuit

The N divider switching to the N+1 divider and N+1 divider switching to N divider will produce a phase shift which is increasing by time .So if N+1 divider for B times at first and N divider for B-A times easily. The signal after dividing will produce a large phase noise, so the best way is mixing two dividers on average.

1.4.1 Decimal calculated frequency divider:

These algorithm is implemented by calculating the integer and decimal frequencies at the same time, which will increase the speed of the process.
In these Algorithm we divider the frequency into two parts.
1) Integer Frequency
2) Decimal Frequency

By calculating the integer and decimal frequency simultaneously we can reduce the error of the clock which will be reduced by adjusting frequency clock frequency dynamically. By using these algoritham we can reduce the number of registers in the hardware. By using these algoritham accuracy of the divider can be reduced.

2. LITERATURE SURVEY

The Serial Peripheral Interface or SPI bus is a synchronous serial data link, a de facto standard, named

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by Motorola, that operates in full duplex mode. It is used for short distance, single master communication, for example in embedded systems, sensors, and SD cards.

Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select lines. Sometimes SPI is called a four-wire serial bus, contrasting with three-, two-, and one-wire serial buses. SPI is often referred to as SSI (Synchronous Serial Interface).

DATA TRANSMISSION

To begin a communication, the bus master first configures the clock, using a frequency less than or equal to the maximum frequency the slave device supports. Such frequencies are typically up to a few MHz.

The master then transmits the logic 0 for the desired chip over the chip select line. A logic 0 is transmitted because the chip select line is active low, meaning its off state is a logic 1; on is asserted with a logic 0. If a waiting period is required (such as for analog-to-digital conversion), then the master must wait for at least that period of time before starting to issue clock cycles.

During each SPI clock cycle, a full duplex data transmission occurs:

- the master sends a bit on the MOSI line; the slave reads it from that same line
- the slave sends a bit on the MISO line; the master reads it from that same line

Transmissions normally involve two shift registers of some given word size, such as eight bits, one in the master and one in the slave; they are connected in a ring. Data is usually shifted out with the most significant bit first, while shifting a new least significant bit into the same register. After that register has been shifted out, the master and slave have exchanged register values. Then each device takes that value and does something with it, such as writing it to memory. If there is more data to exchange, the shift registers are loaded with new data[1] and the process repeats.

Transmissions may involve any number of clock cycles. When there is no more data to be transmitted, the master stops toggling its clock. Normally, it then deselects the slave.

Transmissions often consist of 8-bit words. A master can initiate multiple such transmissions if it wishes/needs. However, other word sizes are also common, such as 16-bit words for touchscreen controllers or audio codecs, like the TSC2101 from Texas Instruments; or 12-bit words for many digital-to-analog or analog-to-digital converters.

Every slave on the bus that has not been activated using its chip select line must disregard the input clock and MOSI signals, and must not drive MISO. The master must select only one slave at a time.

2.1 Comparison between SPI v/s I2C:

Table 2.1: Comparison Between SPI V/S I2C

	I2C	SPI
Originator	Philips (1982)	Motorola (1979)
Plug &Play	Yes	No
Interface type	Serial (2wires)	Serial (3+N wires)
Distance	Short	Short
Application	Multi-MasterRegister -access	Transfer of Data-streams
Protocol Complexity	Low	Lower
Design cost	Low	Lower
Transfer rate	Limited (100&400KHz and 3.4MHz)	Free (nxMHz to 10nxMHz)
Power Consumption	Low(2 pull- up resistors)	Lower

2.1.1 Advantages of SPI over I2C:

- SPI protocol does not have the concept acknowledge, where the I2C protocol have.
- SPI protocol have 4(SI,SO, SCK,SS) bus lines, where I2C have only 2(SCL,SDA) bus lines, so I2C protocol decrease the printed circuit board size.
- SPI protocol has lack of built device addressing,I2C protocol have built in addressing scheme and straight forward.
- SPI protocol have single master, single slave where I2C protocol have multi master, multi slave.
- SPI protocol has less overhead when handling point-to-point communication, where I2C protocol has more overhead when handling point-to-point communication.

2.2 Dividers:

2.2.1 Analog Dividers: In analog dividers suppose if we want 220.12khz frequency but we have crystal of 40MHz,then we separate crystal. In analog dividers if we want frequency 220.123khz but crystal is 40MHz then will use PLL or PLD which will increase size of chip,which will increase the cost.

2.2.2 Digital Divides:

In digital dividers if we need 220.123khz but we have the crystal of 40MHZ then we divide frequency according to the user requirements,we will provide the divider re-configuralable which will reduce the size of divider but also reduce the cost of the divider.

Paper Algorithm:

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The decimal based frequency was calculated by N and N+1 counter which decrease the clock frequency cost rather than using analog divider or crystal oscillatrors. In these method we can reduce the cost rather the using the PLL OR PLD's.

Proposed Algorithm:

It is simple algorithm in which decimal frequency is calculated very accurately .It will reduce the number of the registers which will reduce the power of the circuit.It is simple algorithm, so we can generate re-configurable divider very easily without using much effort.

3. SIMULATION RESULTS

Simulation results shows how the clock divider circuit is implemented using the (INTER INTEGRATED CIRCUIT) IIC protocol.

Here we give the clk,data from the testbench through the bus lines SDA,SCLIN and give it to the IIC slave

Then IIC slave receives the data according to the following steps:

1. Start condition (using both SDA AND SCLIN lines)
2. address of 7 bit.(using SDA line).
3. 8bit R/W (using SDA line).
4. Slave acknowledge (using SDA line).
5. Then master sends data through SDA line.(using SDA line).
6. For each data receiving slave acknowledge.(using SDA line).
7. After completing the data transfer master terminates using stop condition. (using both SDA and SCLIN lines).
8. After receiving the data through the IIC protocol , it is given to the clock divider circuit.

The clock divider circuit produces different frequencies of non integer type (ex:100.54khz,222.23khz)

4. SIMULATION RESULTS DIVIDER(XILINX ISE SIMULATOR)

OUTPUT FOR NON INTEGER CLOCK DIVIDER

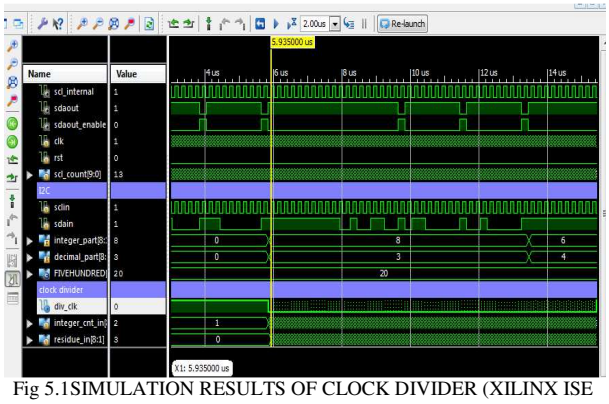

Fig 5.1SIMULATION RESULTS OF CLOCK DIVIDER (XILINX ISE SIMULATOR)

I2C

Input :..... SCLK,SDATA

CLK_DIVIDER

Output: .....Div_clk

Description: This block shows how the clock divider output(div_clk) is produced with the inputs SDATA consists of integer part and decimal part (8.3.....&.....6.4).

OUTPUT FOR NON INTEGER CLOCK DIVIDER

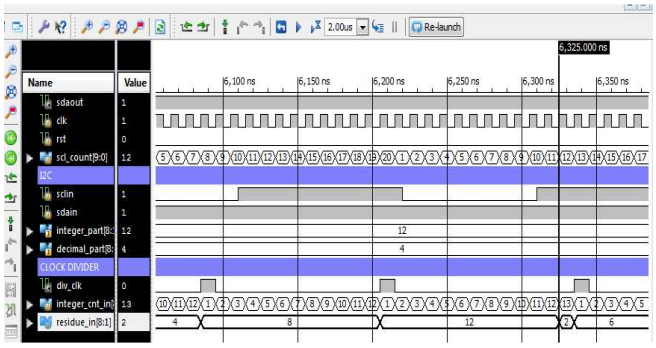

Fig:5.2 SIMULATION RESULTS OF CLOCK DIVIDER (XILINX ISE SIMULATOR)

I2C

Input :..... SCLK,SDATA

CLK_DIVIDER

Output: .....Div_clk

Description: This block shows how the clock divider output(div_clk) is produced with the inputs SDATA consists of integer part and decimal part (12.4).

Here the 12.4khz is produced by taking integerpart (12) in register which counts upto 12 for every cycle

The remaining decimal part(4) is taken in a register which is added with the same decimal part (4) for every clk cycle and so on ...

when the decimal part is greater than 10 (12)as shown in the fig ..then the counter which is counting 12 for every cycle increments to 13 (as shown in fig) leaving the residue(2)in the decimalpart..

OUTPUT FOR NON INTEGER CLOCK DIVIDER

Fig:5.3 SIMULATION RESULTS OF CLOCK DIVIDER (XILINX ISE SIMULATOR)

I2C

Input :..... SCLK,SDATA

CLK_DIVIDER

Output: .....Div_clk

Description: This block shows how the clock divider output(div_clk) is produced with the inputs SDATA consists of integer part and decimal part (9.3).

Here the 9.3khz is produced by taking integerpart (9) in register which counts upto 9 for every cycle

The remaining decimal part(3) is taken in a register which is added with the same decimal part (3) for every clk cycle and so on ...

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when the decimal part is greater than 10 (11)as shown in the fig ..then the counter which is counting 9 for every cycle increments to 10 (as shown in fig) leaving the residue(1)in the decimalpart..

OUTPUT FOR NON INTEGER CLOCK DIVIDER

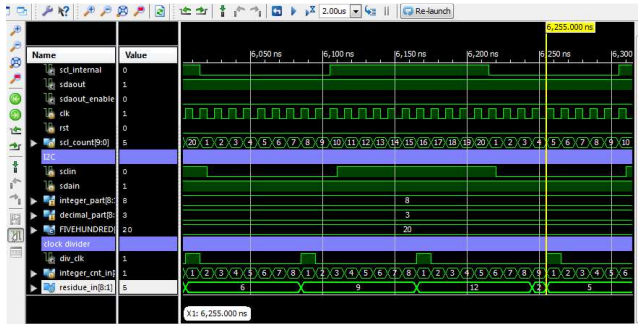

Fig:5.4 SIMULATION RESULTS OF CLOCK DIVIDER (XILINX ISE SIMULATOR)

I2C

Input :..... SCLK,SDATA

CLK_DIVIDER

Output: .....Div_clk

Description: This block shows how the clock divider output(div_clk) is produced with the inputs SDATA consists of integer part and decimal part (8.3).

Here the 8.3khz is produced by taking integerpart (8) in register which counts upto 8 for every cycle

The remaining decimal part(3) is taken in a register which is added with the same decimal part (3) for every clk cycle and so on ...

when the decimal part is greater than 10 (12)as shown in the fig ..then the counter which is counting 8 for every cycle increments to 9 (as shown in fig) leaving the residue(2)in the decimalpart..

RTL Design (.ngr file):

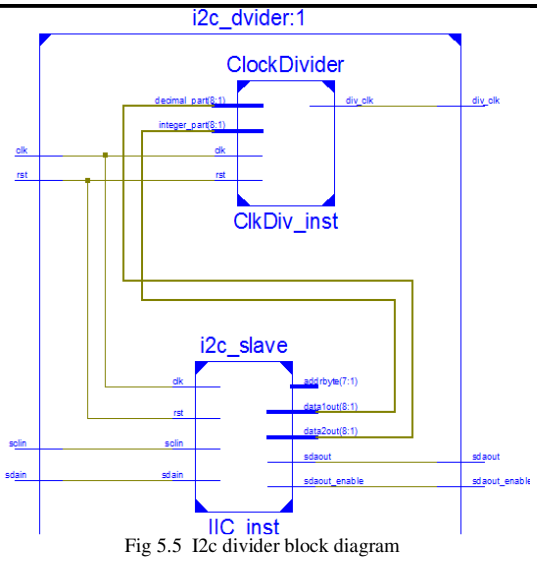

Fig 5.5 I2c divider block diagram

Technical sechematic:

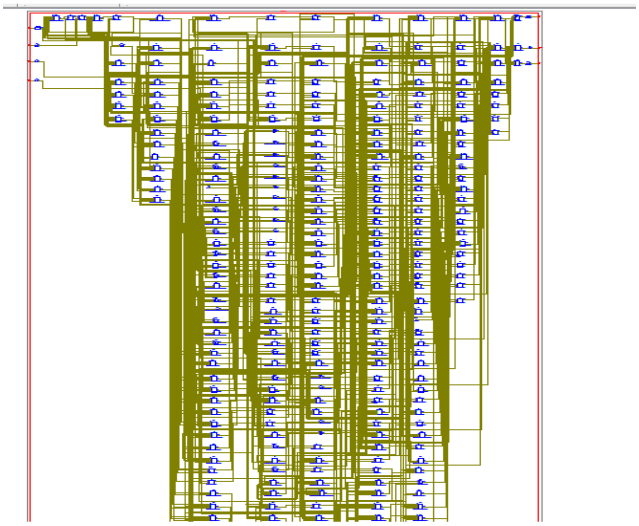

Fig 5.6 I2C divider schematic diagram

Table 5.1 Device Utilization Summary

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	98	207360	0%
Number of Slice LUTs	151	207360	0%
Number of fully used LUT-FF pairs	77	172	44%
Number of bonded IOBs	7	1200	0%
Number of BUFG/BUFGCTRLs	1	32	3%

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Table5.2: COMPARISON TABLE OF BASE PAPER RESULTS AND PROPOSED ALGORITHM RESULTS

Previous Algorithm Results (using SPI protocol) BASE PAPER				Proposed Algorithm Results (using IIC protocol) IMPLEMENTED		
	Used	Available	Utilization	Used	Available	Utilization
Slices	265	3584	7%	151	3584	4.2%
Flip-Flops	335	7168	4%	98	7168	1.3%
LUT's	324	7168	4%	151	7168	2.1%
BOND IOBS	7	141	4%	7	141	4%

5. CONCULSION

Reduced the number of bus lines between the protocols, which will done by introducing I2C protocol. We reduce the number of registers between the frequency divider which will reduce the power. We developed re-configurable divider ,which will reduce the cost of the frequency divider. I2C will reduce the size of the printer circuit board. By used I2C protocol in place of SPI protocol for efficient utilization of the registers and memory This is the one of the good application for less circutry device. we can reduce the number of crystals and size of of printed circuit board and also reduce the cost of the design.

FUTURE SCOPE: If we introduce this frequency divider in mobile phones and we can reduce the number of crystals and size of of printed circuit board and also reduce the cost of the design. Data processing: Laptop, Desktop, Workstation, Server Consumer: Audio/video systems, Consumer electronics (DVD, TV etc.)

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P. SAYANNA received his B.Tech in Srinivas Reddy Institute of Technology, Nizamabad. Completed on 2005.And PG received in Aurora College of Engineering, Bhongiri. Completed on 2012 He is currently working as a Associate Professor, Principal for Diploma polytechnic, Department of ECE In Sudheer Reddy College Of Engineering & Technology (W) Keshapur Road, Bardipur (Mdl); Dichpally, Nizamabad, Telangana. And his Interest Area is VLSI, (VLSI-Low Power, Mixed Signal) Signal Processing, Image Processing, DSP, Embedded System and he Has total 12 years of teaching experience.