International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 4, Issue 3, March 2017)

Low Power Design of Testable Reversible Combinational and Sequential Circuits

Venkatramana Gembali
Electronics & Communication Engineering
NIT-Andhrapradesh

Abstract: **In this Project, we propose the design of two vectors testable sequential circuits based on conservative logic gates. The proposed sequential circuits based on conservative logic gates outperform the sequential circuits implemented in classical gates in terms of testability. Any sequential circuit based on conservative logic gates can be tested for classical unidirectional stuck-at faults using only two test vectors. The two test vectors are all 1s, and all 0s. The designs of two vectors testable latches, master-slave flip-flops, double edge triggered (DET) flip-flops and 4x4 multiplier are presented. The importance of the proposed work lies in the fact that it provides the design of reversible sequential circuits completely testable for any stuck-at fault by only two test vectors, thereby eliminating the need for any type of scan-path access to internal memory cells.**

Keywords: **QCA, nano scale, CMOS, Conservative, Circuits**

1. INTRODUCTION

CONSERVATIVE logic is a logic family that exhibits the property that there are an equal number of 1s in the outputs as there are in the inputs. Conservative logic can be reversible in nature or may not be reversible in nature. Reversibility is the property of circuits in which there is one to-one mapping between the inputs and the output vectors, that is for each input vector there is a unique output vector and vice-versa. Conservative logic is called reversible conservative logic when there is a one-to-one mapping between the inputs and the outputs vectors along with the property that there is equal number of 1s in the outputs as in the inputs. Conservative logic circuits are not reversible, if one-to-one mapping between the inputs and the outputs vectors is not preserved.

Researchers have proved that if the computation is performed in an irreversible manner, each bit of information lost will produce KTln2 Joules of heat energy. From a thermodynamic point of view, it is also proved that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way. There are emerging nanotechnologies, such as quantum-dot cellular automata (QCA) computing, optical computing, and superconductor flux logic family, etc., where the energy dissipated due to information destruction will be a significant factor of the overall heat dissipation of the system. Thus, one of the primary motivations for adopting reversible logic lies in the fact that it can provide a logic design methodology for designing ultralow power circuits beyond KTln2 limit for those emerging nanotechnologies in which the energy dissipated due to information destruction will be a significant factor of the overall heat dissipation. Further, QCA is one of the emerging nanotechnologies in which it is possible to implement reversible logic gates.

QCA makes it possible to achieve circuit densities and clock frequencies beyond the limits of existing CMOS technology. In QCA, computing logic states of 1 and 0 are represented by the position of the electrons inside the QCA cell. Thus, when the bit is flipped from 1 to 0 there is no actual discharging of the capacitor as in conventional CMOS. Hence, QCA does not have to dissipate all its signal energy during transition. Further, propagation of the polarization from one cell to another is because of interaction of the electrons in adjacent QCA cells. As there is no movement of electrons from one QCA cell to the other, there is no current flow. Thus, QCA has no dissipation in signal propagation. Therefore, QCA has significant advantage compared to CMOS technology in terms of power dissipation. Due to high error rates in nano-scale manufacturing, QCA and other nanotechnologies target reducing device error rates.

1.1 Back Ground

A conservative logic gate is a multiple-output logic element in which the number of 1s at the inputs is equal to that of the corresponding outputs. According to [7] and [8], a conservative logic circuit can be considered as a directed graph whose nodes are conservative logic gates, and the edges are wires of arbitrary lengths. The FO at the output is not allowed in conservative logic circuits. A conservative logic network can be reversible in nature if the one-to-one mapping is maintained between the inputs and the outputs, while it will be irreversible in nature if one-to-one mapping is not preserved. Researchers in [7], [9], and [10] have proved that:

1) in the event of unidirectional stuck-at-faults in a conservative logic network, either the number of 1s in its output set will differ from the number of 1s in its input set, or the output set is correct and
2) in a conservative logic network the two vector test sets, all 1s and all 0s, provide 100% coverage for unidirectional stuck-at faults. Any stuck-at-1 fault in the conservative logic circuit can be detected by setting all inputs to 0s followed by subsequent checking of the outputs for the presence of any 1s. Any stuck-at-0 faults can be detected by setting all inputs to 1s followed by subsequent checking of outputs for the presence of any 0s. The comprehensive proofs can be referred in [7], [9], and [10]

1.2 Conservative Reversible Fredkin Gate

The Fredkin gate is a popularly used reversible conservative logic gate, first proposed by Fredkin and Toffoli

International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 4, Issue 3, March 2017)

in [8]. The Fredkin gate shown in Fig. 1 can be described as a mapping (A, B, C) to (P = A, Q = A'B + AC, R = A B + A'C),
where A, B, C are the inputs and P, Q, R are the outputs respectively. The truth table for the Fredkin gate is illustrated in [3], which demonstrates that Fredkin gate is reversible and conservative in nature, that is, it has unique input and output mapping and also has the same number of 1s in the outputs as in the inputs.

Researchers have proved that if the computation is performed in an irreversible manner, each bit of information lost will produce KTln2 Joules of heat energy. From a thermodynamic point of view, it is also proved that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way. There are emerging nanotechnologies, such as quantum-dot cellular automata (QCA) computing, optical computing, and superconductor flux logic family, etc., where the energy dissipated due to information destruction will be a significant factor of the overall heat dissipation of the system. Thus, one of the primary motivations for adopting reversible logic lies in the fact that it can provide a logic design methodology for designing ultralow power circuits beyond KTln2 limit for those emerging nanotechnologies in which the energy dissipated due to information destruction will be a significant factor of the overall heat dissipation.

2. LITERATURE REVIEW

2.1. Reversible Logic-Based Concurrently Testable Latches for Molecular QCA.

Nanotechnologies, including molecular quantum dot cellular automata (QCA), are susceptible to high error rates. In this paper, we present the design of concurrently testable latches (D latch, T latch, JK latch, and SR latch), which are based on reversible conservative logic for molecular QCA. Conservative reversible circuits are a specific type of reversible circuits, in which there would be an equal number of 1's in the outputs as there would be on the inputs, in addition to one-to-one mapping. Thus, conservative logic is parity-preserving, i.e., the parity of the input vectors is equal to that of the output vectors. The fault patterns in the conservative reversible Fredkin gate due to a single missing/additional cell defect in molecular QCA. If there is a fault in the molecular QCA implementation of Fredkin gate, there is a parity mismatch between the inputs and the outputs, otherwise the inputs parity is the same as outputs parity. Any permanent or transient fault in molecular QCA can be concurrently detected if implemented with the conservative Fredkin gate. The design of QCA layouts and the verification of the latch designs using the QCA Designer and the HDLQ tool are presented. The use of conservative reversible logic based on Fredkin gate to design concurrently testable sequential circuits for molecular QCA. The proposed concurrent testing methodology is based on parity-preserving property of Fredkin gate, and is beneficial for both permanent and transient faults that results in parity mismatch between inputs and outputs.

2.2. Constructing Online Testable Circuits Using Reversible Logic

With the advent of nanometer technology, circuits are more prone to transient faults that can occur during its operation. Of the different types of transient faults reported in the literature, the single-event upset (SEU) is prominent. Traditional techniques such as triple-modular redundancy (TMR) consume large area and power. Reversible logic has been gaining interest in the recent past due to its less heat dissipation characteristics. This paper proposes the following: (1) a novel universal reversible logic gate (URG) and a set of basic sequential elements that could be used for building reversible sequential circuits, with 25% less garbage than the best reported in the literature; (2) a reversible gate that can mimic the functionality of a lookup table (LUT) that can be used to construct a reversible field-programmable gate array (FPGA); and (3) automatic conversion of any given reversible circuit into an online testable circuit that can detectonline any single-bit errors, including soft errors in the logic blocks, using theoretically proved minimum garbage, which is significantly lesser than the best reported in the literature. This paper has proposed several reversible circuits for realizing both combinational and sequential elements of a given digital circuit. A URG, which is shown to be advantageous for synthesizing multivalued reversible logic, was presented. This paper has also proposed a reversible gate that can mimic the functionality of a two-input LUT, thus enabling the memory less realization of LUTs. This can be used as a programmable logic block in modern field-programmable gate array architectures. This paper has presented efficient realizations of reversible sequential elements. The proposed designs lead to a 25% reduction in garbage and a lesser number of 3 × 3 reversible gates when compared with the best reported in the literature. This paper has also proposed a methodology that automatically converts any circuit into an online testable reversible circuit with theoretically proved minimum garbage. The resultant testable circuit can detect online any singlebit errors in the logic blocks. An important advantage of the technique is that the design of a given reversible circuit need not be changed for the purpose of adding testability feature to it. This paper has discussed the construction of hierarchical multi modular online testable reversible circuits.

3. PROPOSED SYSTEM

In this project, we propose the design of testable sequential circuits based on conservative logic gates. The proposed technique will take care of the fan-out (FO) at the output of the reversible latches and can also disrupt the feedback to make them suitable for testing by only two test vectors, all 0s and all 1s. In other words, circuits will have feedback while executing in the normal mode. However, in order to detect faults in the test mode, our proposed technique will disrupt

International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 4, Issue 3, March 2017)

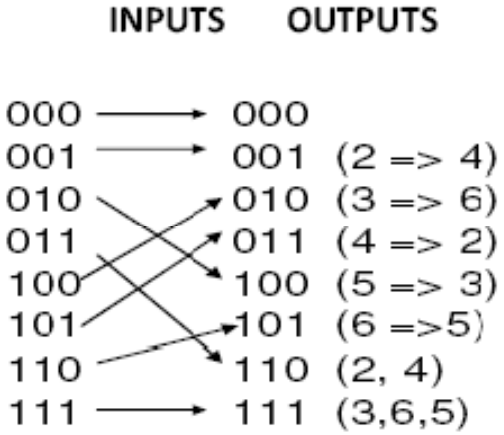
feedback to make technique is extended toward the design of two vectors testable master-slave flip-flops and double edge triggered (DET) flip-flops. Thus, our work is significant because we are providing the design of reversible sequential circuits completely testable for any unidirectional stuck-at faults by only two test vectors. The reversible design of the DET flip-flop is proposed for the first time in the literature and also designed 4x4 multiplier by using HNG and Peres Gates.

4. DESIGN OF REVERSIBLE LOGIC GATES

4.1 BASIC GATES - BASIC REVERSIBLE GATES USED

1. 4*4 IG Gate
2. 3*3 F2G Gate
3. 3*3 FG Gate
4. 3*3 NG Gate
5. 3*3 TG Gate
6. 2*2 FEYNMAN Gate
7. 4*4 HNG Gate

Reversible circuits or gates are those which have one-to-one mapping between vectors of inputs and outputs. This allows the vector of output states to be used to reconstruct the vector of input states. Reversible logic can be obtained by the following relation as shown below:



4.1.1 IG GATE

This paper includes a 4*4 parity preserving reversible gate, IG[11], as depicted in Fig. The gate is one-through, which means one of the input variables is also used as the output variable.

Fig 1: 4*4 IG Gate.

The truth table of this IG gate is shown in Table.1., which shows that this gate allows to uniquely determine the input pattern corresponding to particular output pattern. As the Reversible IG gate is parity preserving. This property can be verified by comparing the input parity **A** XOR **B** XOR **C** XOR **D** to the output parity **P** XOR **Q** XOR **R** XOR **S**. This Reversible IG gate is universal as it can be used to implement any arbitrary Boolean function.

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

Table I: Truth Table For Parity Preserving IG GATE.

4.1.2 F2G GATE

A 3*3 Double Feynman gate is depicted in Fig. The input vector is I (A, B, C) and the output vector is O (P, Q,R). The outputs are defined as

P = A
Q = A XOR **B**
R = A XOR **C**

Then the Quantum cost of double Feynman gate is 2.

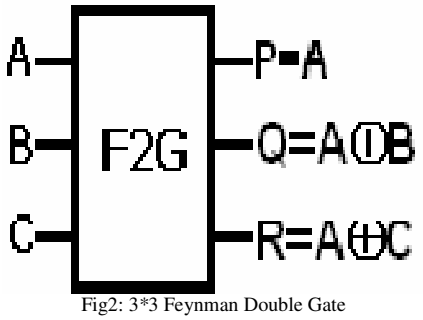


Fig2: 3*3 Feynman Double Gate

Feynman Double gate is used as the fault tolerant copying gate when the input lines B and C are set to some constants may be '0' or '1' or as a combination of both '0' and '1'.

International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 4, Issue 3, March 2017)

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Table II: Truth Table for Feynman Double Gate.

4.1.3 FREDKIN GATE

Fredkin gate shown in Fig, is a (3, 3) reversible gate which realizes P, Q and R where (A,B,C) is the input vector and (P, Q, R) is the output vector. As Fredkin gate is designed to be its own inverse, it is also a self-reversible gate. It is a conservative gate because the hamming weight of an input is same as its output.

This gate uses the input 'A' as the control input, i.e., if A = '0', then the outputs have to be simply duplicates of the inputs; else A = '1', and the output must have interchange of the B and C input lines.

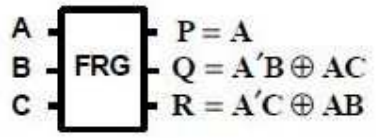


Fig 3: 3*3 Fredkin Gate

Fredkin gate also named as FG gate which is known as a universal reversible gate, i.e., This gate is used to construct the basic logic gates or blocks like AND, OR, NOT reversible gates. Also the other gates like NAND, NOR, XOR and XNOR reversible gates can be constructed by setting some of the inputs prior to use.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Table III: Truth Table for FRG Gate Implementation of Fredkin Gate

We can save area by using transmission gates in the design of any circuits and power dissipation very much reduced because transmission gates themselves do not consume any power; simply it transfers input data to output data. The implementation is shown in Fig 3(a).

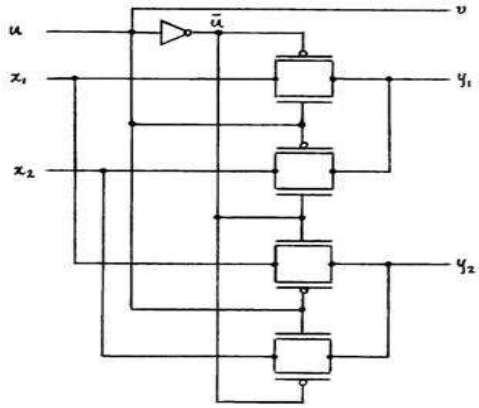


Fig 3(a) Fredkin gate implementation by using transmission gates

4.1.4 NEW TG GATE

The proposed New TG gate is another gate that acts as the input value duplicator. It is basically a 3*3 reversible gate. This gate is represented as shown in Fig., the outputs are defined as

P = A
Q = B
R = AB XOR **C**

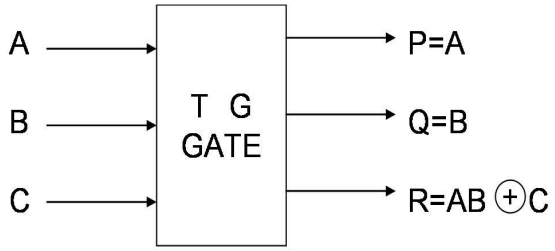


Fig 4: 3*3 New TG GATE

The truth table of the 3*3 New TG gate is as provided in the Table. IV. This satisfies the conditions imposed for reversibility.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Table IV: Truth Table of New TG Gate

International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 4, Issue 3, March 2017)

4.1.5 NEW GATE

The New Gate is as shown in Fig. is another gate which implements all the basic operations like a universal gate i.e., all other gates can be derived from this gate using the inputs and outputs in either directions to implement any logic circuit. This gate is represented as shown in Fig. the outputs are defined as

P = A
Q = AB XOR **C**
R = A'C' XOR **B'**

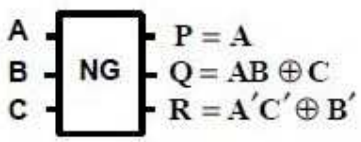


Fig 5: 3*3 New Gate

The truth table of NG gate that satisfies all of the parity preserving properties required for reversibility is provided in Table V.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	1	0	0

Table V: Truth Table of New Gate

4.1.6 FEYNMAN GATE

Fig. shows a 2 x 2 feynman gate. The input vector is I (A, B,) and the output vector is O (P, Q,) and the relation between input and output is defined by
P=A,Q=A XOR B.

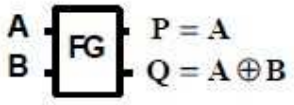


Fig 6 Feynman Gate

4.1.7 HNG GATE

Fig. shows a 4 x 4 HNG gate [5]. The input vector is I (A, B, C,D) and the output vector is O (P, Q, R,S) and the relation between input and output is defined by
P=A,Q=B,R=A XOR B XORC,S=(A X OR B).C XOR AB XOR D.

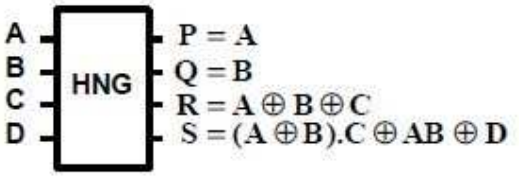


Fig 7 HNG Gate

4.2 Types of reversible logic

Venn diagram for various reversible gates is depicted in figure

Reversible: There is a one to one mapping between inputs and outputs.

Conservative: The same number of one's is in the output as in the input.

The most widely used reversible gate is a fredkin gate, because it has the properties of Reversibility, Conservative and the same number of inputs and outputs.

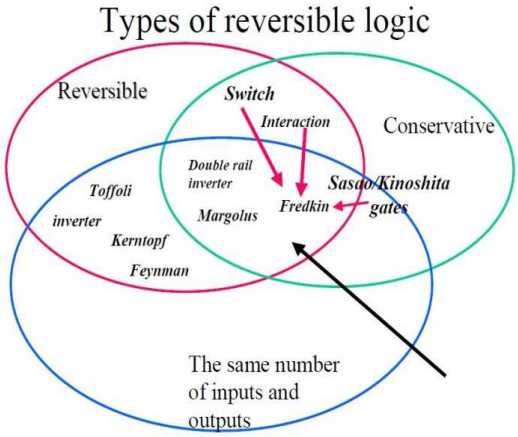


Fig 8 venn diagram for various reversible gates

A reversible logic circuit should have the following features.

- Use minimum number of reversible gates.
- Use minimum number of garbage outputs.
- Use minimum constant inputs.

5. DESIGN METHODOLOGY

5.1 DESIGN OF TESTABLE REVERSIBLE LATCHES

Reversible logic is becoming very popular in recent years because of its ability to reduce power dissipation. Reversible logic circuits are very much needed for construction of quantum arithmetic components and in applications like low power digital design, DNA computing and nano technology. In 1960 R.Landauer explained that circuits and systems constructed using irreversible hardware results in energy dissipation due to information loss.

International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 4, Issue 3, March 2017)

According to Landauer"s principle, the loss of one bit of information dissipates kTln2 joules of energy where k is the Boltzmann"s constant and T is the absolute temperature at which the operation is performed [1]. Later Bennett, in 1973, showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits.

A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. Reversible logic circuits are constructed using Reversible logic gates. Reversible circuits produce unique output vector from each input vector and inputs can be reconstructed from output. Reversible logic circuits should be designed using minimum number of logic gates. Fan-out and loops are not allowed in reversible logic circuits [3]. But fan-out and feedback can be achieved by using additional gates.

The performance of the circuit is decided based on the following parameters [4,5,7].

(i)**Garbage outputs:** The number of unused outputs present in the reversible logic circuit.

(ii)**Number of reversible gates:** Total number of reversible gates used in the circuit.

(iii)**Delay:** Maximum number of unit delay gates in the path of propagation of inputs to outputs. It represents number of reversible gates used between the primary inputs and the outputs of a reversible logic circuit.

(iv)**Constant inputs:** The number of inputs which are maintained constant at 0 or 1 in order to get the required function. They are necessary to synthesize a reversible function.

(v)**Quantum cost:** The number of 1x1 or 2 x 2 reversible logic gates used in the quantum equivalent of the reversible circuit.

The synthesis of a reversible logic circuit should have following optimization parameters [4-18]:

1. Minimum number of gates
2. Minimum number of garbage outputs
3. Minimum number of constant inputs
4. Minimum delay

Decimal addition plays an important role in many applications like microprocessors and in other future computing circuits. Therefore circuits designed to perform decimal addition using binary methods must be fast and it should include the required correction to produce accurate decimal sum. The present paper proposes an optimized Carry Select BCD adder using minimum number of reversible logic gates and it produces least number of garbage outputs compared to other existing circuits and therefore it can be used to build more complex arithmetic circuits using reversible logic gates.

The characteristic equation of the D latch can be written as $Q^+ = D \cdot E + \bar{E} \cdot Q$. In the proposed work, enable (E) refers to the clock and is used interchangeably in place of clock. When the enable signal (clock) is 1, the value of the input D is reflected at the output that is $Q^+ = D$. While, when E = 0 the latch maintains its previous state, that is $Q^+ = Q$. The reversible Fredkin gate has two of its outputs working as 2:1 Muxes, thus the characteristic equation of the D latch can be mapped to the Fredkin gate (F).

Fig. shows the realization of the reversible D latch using the Fredkin gate. But FO is not allowed in conservative reversible logic. Moreover, the design cannot be tested by two input vectors all 0s and all 1s because of feedback, as the output Q would latch 1 when the inputs are toggled from all 1s to all 0s and could be misinterpreted as stuck-at-1 fault.

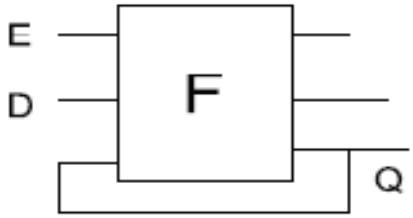


Fig. 9: Fredkin gate based D latch.

In this paper, we propose to cascade another Fredkin gate to output Q as shown in Fig. The design has two control signals, C1 and C2. The design can work in two modes: 1) normal mode and 2) test mode.

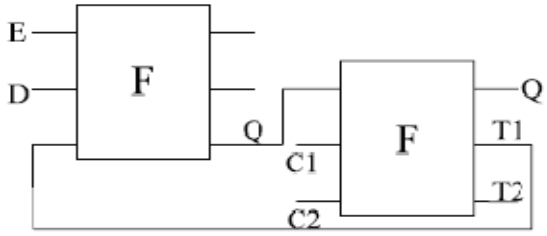


Fig. 10: Fredkin gate based D latch with control signals C1 and C2.

5.1.1 Normal Mode

The normal mode is shown in Fig. in which we will have C1C2 = 01 and we will have the design working as a D latch without any fan-out problem.

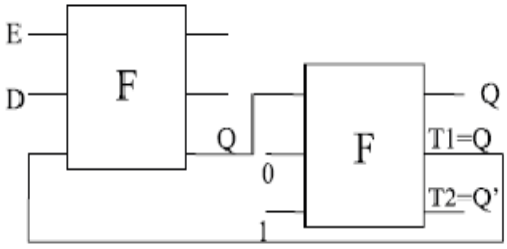


Fig. 11: Fredkin gate based D Latch in normal mode: C1 = 0 and C2 = 1.

5.1.2 Test Mode (Disrupt the Feedback)

In test mode, when C1C2 = 00 as shown in Fig. it will make the design testable with all 0s input vectors as output T1 will become 0 resulting in making it testable with all 0s input vectors. Thus, any stuck-at-1 fault can be detected.

International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 4, Issue 3, March 2017)

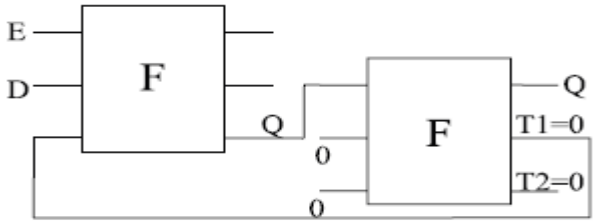


Fig. 12: Fredkin gate based D latch in test mode for stuck-at-1 fault: C1=0 and C2=0

When C1C2 = 11 as shown in Fig. the output T1 will become 1 and the design will become testable with all 1s input vectors for any stuck-at-0 fault. It can seen from above that C1 and C2 will disrupt the feedback in test mode, and in normal mode will take care of the fanout. Thus, our proposed design works as a reversible D latch and can be tested with only two test vectors, all 0s and all 1s, for any stuck-at fault by utilizing the inherent property of conservative reversible logic.

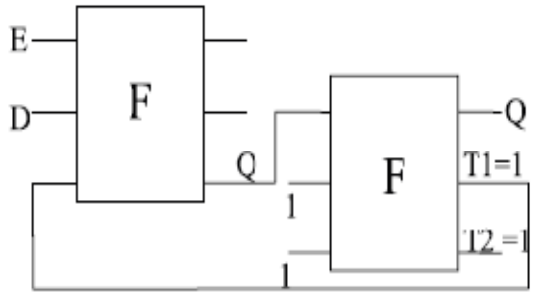


Fig.13: Fredkin gate based D latch in test mode for stuck-at-0 fault: C1=1 and C2=1

5.2 DESIGN OF TESTABLE NEGATIVE ENABLE D LATCH

A negative enable reversible D latch will pass the input D to the output Q when E = 0; otherwise maintains the same state. The characteristic equation of the negative enable D latch is Q+ = D·E' +E·Q. This characteristic equation of the negative enable reversible D latch can be mapped on the second output of the Fredkin gate as shown in Fig. the second Fredkin gate in the design take cares of the FO. The second Fredkin gate in the design also helps in making the design testable by two test vectors, all 0s and all 1s, by breaking the feedback based on control signals C1 and C2 as illustrated above for positive enable reversible D latch.

The negative enable D latch is helpful in the design of testable reversible master-slave flip-flops. This is because as it can work as a slave latch in the testable reversible master-slave flip-flops in which no clock inversion is required. The details of which are discussed in the section describing reversible master-slave flip-flops.

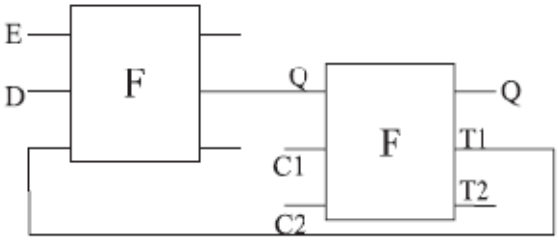


Fig 13: Fredkin gate-based negative enable testable D latch.

5.3 DESIGN OF TESTABLE MASTER-SLAVE FLIP-FLOPS

In the existing literature, the master-slave strategy of using one latch as a master and the other latch as a slave is used to design the reversible flip-flops [13]. In this paper, we have proposed the design of testable flip-flops using the masterslave strategy that can be tested for any stuck-at faults using only two test vectors, all 0s and all 1s. Fig. shows the design of the master-slave D flip-flop in which we have used positive enable Fredkin gate-based testable D latch as the master latch, while the slave latch is designed from the negative enable Fredkin gate-based testable D latch. The testable reversible D flip-flops has four control signals mC1,mC2, sC1, and sC2. mC1 and mC2 control the modes for the master latch, while sC1 and sC2 control the modes for the slave latch. In the normal mode, when the design is working as a master-slave flip-flop the values of the controls signals will be mC1 = 0 and mC2 = 1, sC1 = 0 and sC2 = 1 (as similar to values of the control signals C1 and C2 earlier described for the testable D latches).

In the test mode

- To make the design testable with all 0s input vectors for any stuck-at-1 fault, the values of the controls signals will be mC1 = 0 and mC2 = 0, sC1 = 0 and sC2 = 0. This will make the outputs mT 1 and sT 1 as 0, which results in breaking the feedback and the design becomes testable with all 0s input vectors for any stuck-at-1 fault.
- To make the design testable with all 1s input vectors for any stuck-at-0 fault, the values of the control signals will be mC1 = 1 mC2 = 1, sC1 = 1, and sC2 = 1. This will result in outputs mT 1 and sT 1 having a value of 1, breaking the feedback and resulting in the design testable with all 1s input vectors for any stuck-at-0 fault.

The other type of master-slave flip-flops, such as the testable master-slave T flip-flop, testable master-slave JK flip-flop, and testable master-slave SR flip-flop can be designed similarly in which master is designed using the positive enable corresponding latch, while the slave is designed using the negative enable Fredkin gate-based D latch. For example, in the design of master-slave T flip-flop, the master is designed using the positive enable T latch, while the slave is designed with the negative enable D latch.

International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 4, Issue 3, March 2017)

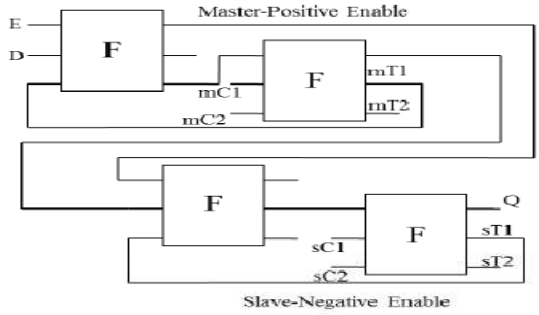


Fig. 14: Fredkin gate-based testable reversible master-slave D flip-flop

5.4 DESIGN OF TESTABLE REVERSIBLE DET FLIP-FLOPS

The DET flip-flop is a computing circuit that samples and stores the input data at both the edges, that is at both the rising and the falling edge of the clock. The masterslave strategy is the most popular way of designing the flip flop. In the proposed work, E refers to the clock and issued interchangeably in place of clock. In the negative edge triggered master-slave flip-flop when E = 1 (the clock is high), the master latch passes the input data while the slave latch maintains the previous state. When E = 0 (the clock is low), the master latch is in the storage state while the slave latch passes the output of the master latch to its output. Thus, the flip-flop does not sample the data at both the clock levels and waits for the next rising edge of the clock to latch the data at the master latch.

In order to overcome the above problem, researchers have introduced the concept of DET flip-flops, which sample the data at both the edges. Thus, DET flip-flops can receive and sample two data values in a clock period thus frequency of the clock can be reduced to half of the master-slave flip flop while maintaining the same data rate. The half frequency operations make the DET flip flops very much beneficial for low power computing as frequency is proportional to power consumption in a circuit. The DET flip-flop is designed by connecting the two latches, viz., the positive enable and the negative enable in parallel rather than in series. The 2:1 MUX at the output transfer the output from one of these latches which is in the storage state (is holding its previous state).The equivalent testable reversible design of the DET flip flop is proposed in this paper and is shown in Fig.

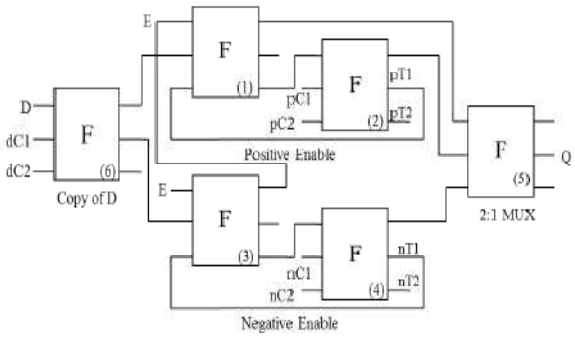


Fig. 15 Fredkin gate-based DET flip-flop.

In the proposed design of testable reversible DET flip-flop, the positive enable testable reversible D latch and the negative enable testable reversible D latch are arranged in parallel. The Fredkin gates labeled as 1 and 2 forms the positive enable testable D latch, while the Fredkin gates labeled as 3 and 4 forms the negative enable testable D latch. In reversible logic FO is not allowed so the Fredkin gate labeled as 6 is used to copy the input signal D. The Fredkin gate labeled as 5 works as the 2:1 MUX and transfer the output from one of these testable latches (negative enable D latch or the positive enable D latch) that is in the storage state (is holding its previous state) to the output Q. In the proposed design of testable reversible DET flip-flop, pC1 and pC2 are the controls signals of the testable positive enable D latch, while nC1 and nC2 are the control signals of the testable negative enable D latch. Depending on the values of the pC1, pC2, nC1, and nC2, the testable DET flip-flops work either in normal mode or in the testing mode.

5.4.1 Normal Mode

The normal mode of the DET flip-flop is illustrated in Fig. in which the pC1 = 0, pC2 = 1, nC1 = 0, and nC2 = 1. The pC1 = 0, pC2 = 1 help in copying the output of the positive enable D latch thus avoiding the FO while the nC1 = 0 and nC2 = 1 help in copying the output of the negative enable D latch thus avoiding the FO.

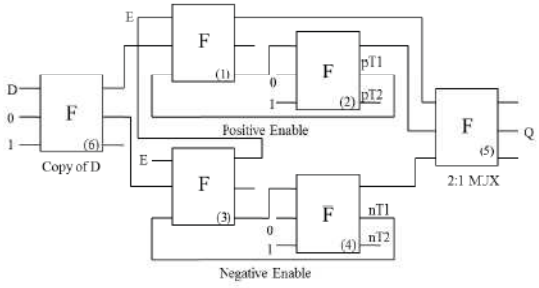


Fig.16 Normal mode

5.4.2 Test Mode

5.4.2(A)All 1's Test Vectors

This mode is illustrated in Fig. in which control signals will have value as pC1 = 1, pC2 = 1, nC1 = 1, and nC2 = 1. The pC1 = 1 and pC2 = 1 help in breaking the feedback of the positive enable D latch, while the nC1 = 1 and nC2 = 1 help in breaking the feedback of the negative enable D latch. This makes the design testable by all 1s test vector for any stuck-at-0 fault.

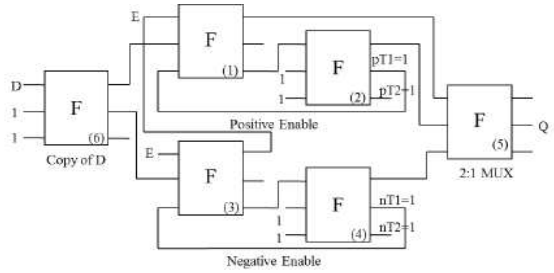


Fig. 17 Test mode for stuck-at-0 fault

International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 4, Issue 3, March 2017)

5.4.2(B) All 0's Test Vectors

This mode is illustrated in Fig. in which the control signals will have value as pC1 = 0, pC2 = 0, nC1 = 0, and nC2 = 0. The pC1 = 0 and pC2 = 0 help in breaking the feedback of the positive enable D latch, while the nC1 = 0 and nC2 = 0 help in breaking the feedback of the negative enable D latch. This makes the design testable by all 0s test vector for any stuck-at-1 fault.

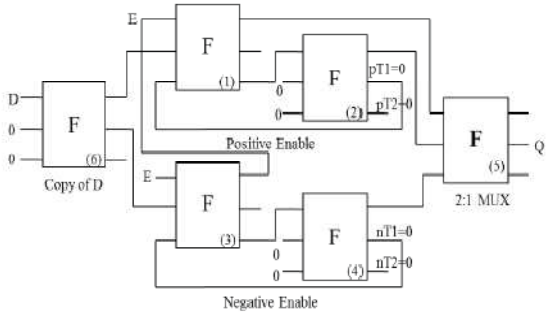


Fig. 18 Test mode for stuck-at-1 fault.

5.5 DESIGN OF 4x4 MULTIPLIER USING PERES AND HNG GATES

A Novel Reversible Multiplier Circuit Using HNG gates: The operation of the 4x4 multiplier is depicted in Fig. It consists of 16 partial product bits of the form $x_i.y_i$.

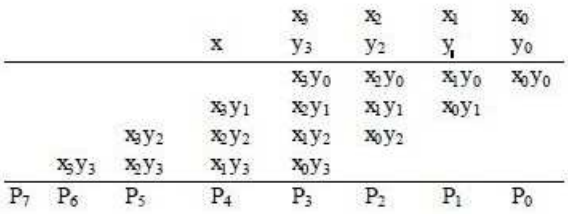


Fig 19 Partial products in a 4x4 multiplication

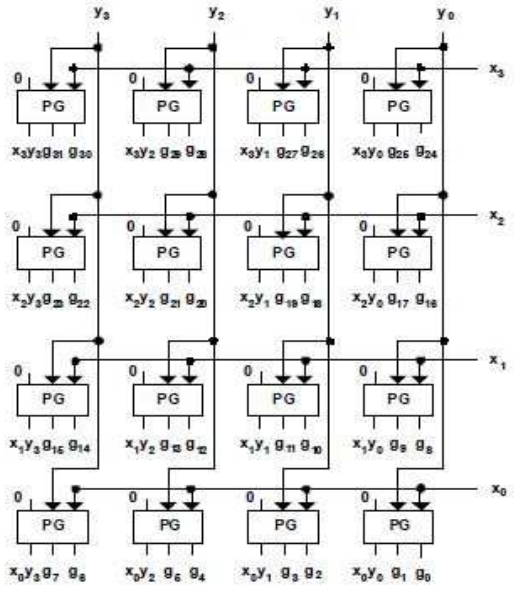


Fig. 20: Reversible partial products generation circuit using Peres gates

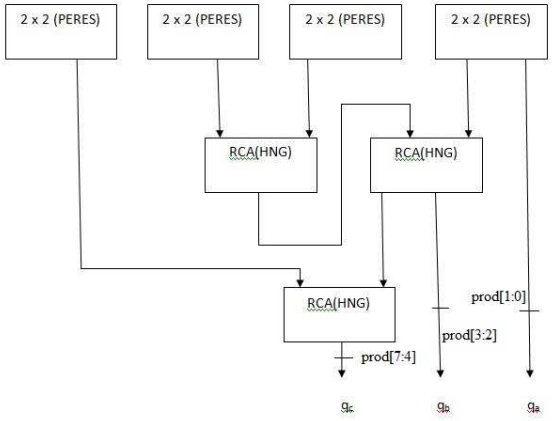


Fig.21: 4x4 reversible multiplier circuit using HNG gates and Peres gates

Our proposed reversible 4x4 multiplier circuit has two parts. First, the partial products are generated in parallel using Peres gates as shown in Fig. Then, the addition is performed as shown in Fig.

The basic cell for such a multiplier is a full adder (FA) accepting three bits. We use HNG gates as reversible full adder which is depicted in Fig.

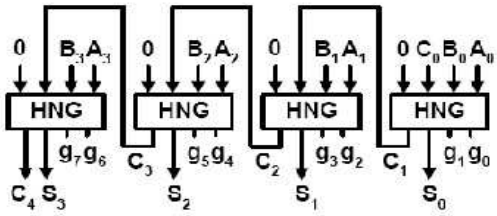


Fig .22: Ripple carry adder by using HNG Gate

The proposed reversible multiplier circuit uses three reversible HNG full adders.

The only difference between partial products generation block in our design with the existing designs is the use of Peres gates instead of Fredkin gates. We use it because the Perse gates have less logical calculation and less quantum cost than the Fredkin gates.

6. SIMULATION RESULTS

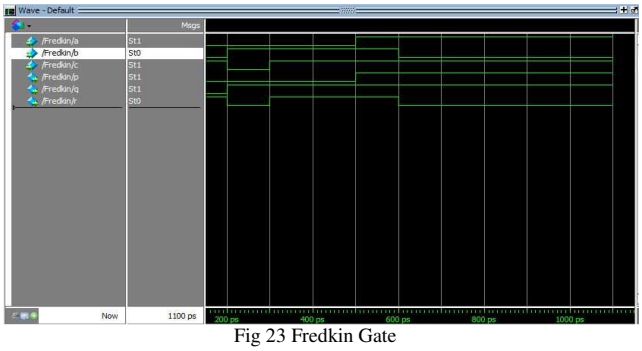


Fig 23 Fredkin Gate

International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 4, Issue 3, March 2017)

When Control signal is 0, the output will be same as input values.
When Control signal 1, the inputs b & c will be swapped and transmitted.

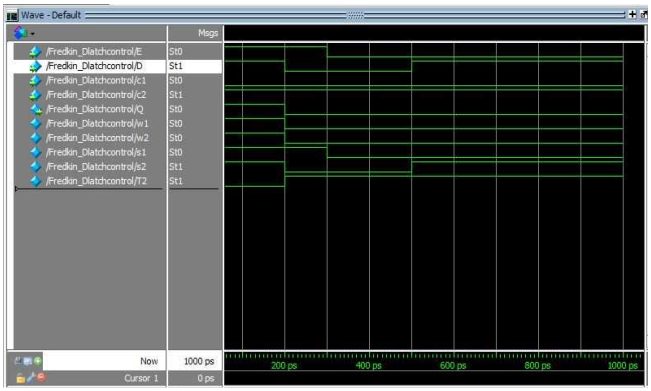


Fig 24 Fredkin Gate Based D Latch with Control Signals C1=0 and C2=1

When the enable signal (clock) is 1, Q^+ =D.
When the enable signal (clock) is 0, Q^+ =Q.

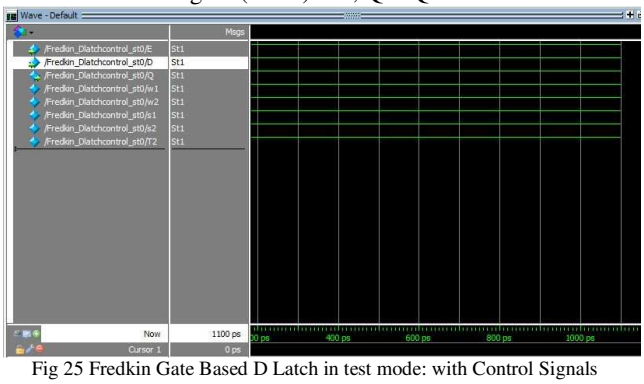


Fig 25 Fredkin Gate Based D Latch in test mode: with Control Signals C1=1and C2=1

In the above case by giving data input and enable signal as 1, we will check for any zero in the output side. Thus, any stuck-at-0 fault can be detected.

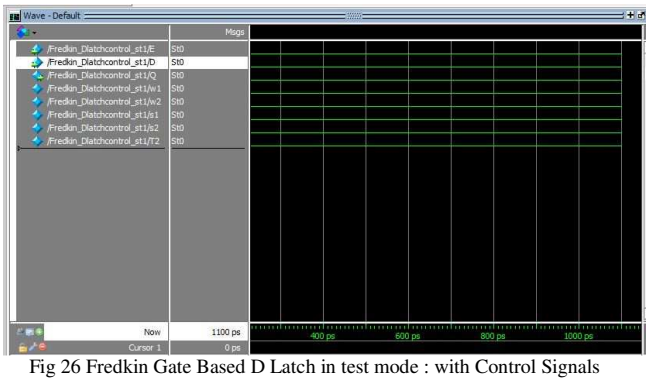


Fig 26 Fredkin Gate Based D Latch in test mode : with Control Signals C1=0and C2=0

In the above case by giving data input and enable signal as 0, we will check for any 1 in the output side. Thus, any stuck-at-1 fault can be detected.

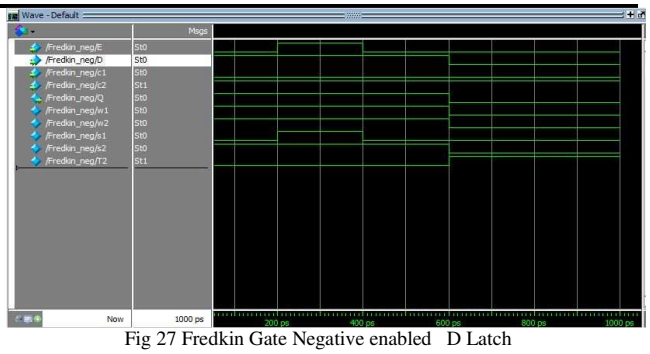


Fig 27 Fredkin Gate Negative enabled D Latch

When the enable signal (clock) is 0, Q^+ =D.
When the enable signal (clock) is 1, Q^+ =Q.

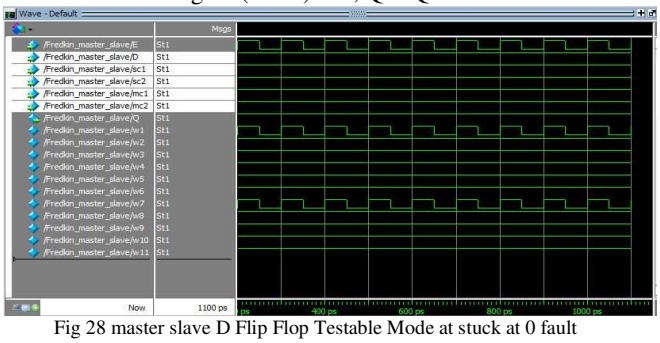


Fig 28 master slave D Flip Flop Testable Mode at stuck at 0 fault

In the above case by giving data input and enable signal as 1 and control signals mc_1,mc_2,sc_1,sc_2 as 1 we will check for any 0 in the output side. Thus, any stuck-at-0 fault can be detected.

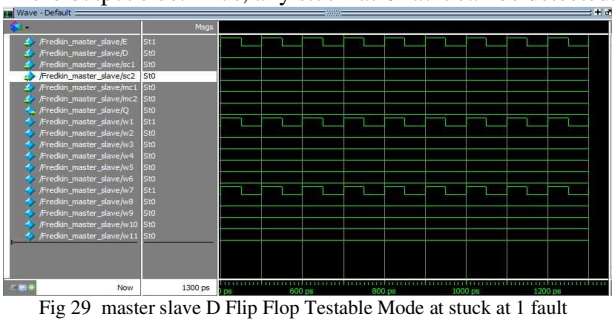


Fig 29 master slave D Flip Flop Testable Mode at stuck at 1 fault

In the above case by giving data input and enable signal as 0 and control signals mc_1,mc_2,sc_1,sc_2 as 0 we will check for any 1 in the output side. Thus, any stuck-at-1 fault can be detected.

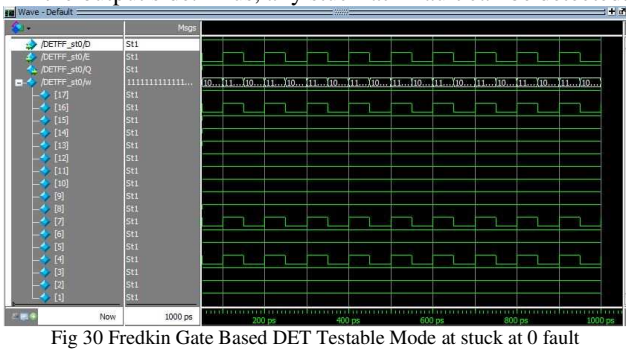


Fig 30 Fredkin Gate Based DET Testable Mode at stuck at 0 fault

International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 4, Issue 3, March 2017)

In the above case by giving data input and enable signal as 1, we will check for any zero in the output side. Thus, any stuck-at-0 fault can be detected.

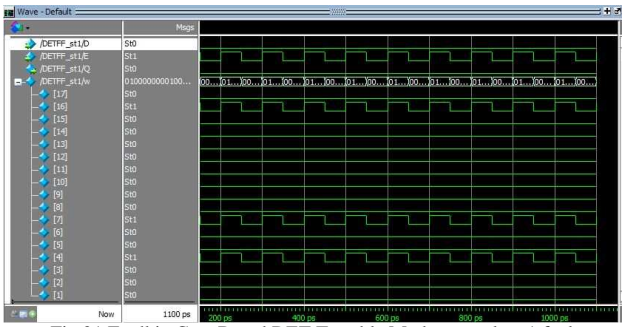


Fig 31 Fredkin Gate Based DET Testable Mode at stuck at 1 fault

In the above case by giving data input and enable signal as 0, we will check for any 1 in the output side. Thus, any stuck-at-1 fault can be detected.

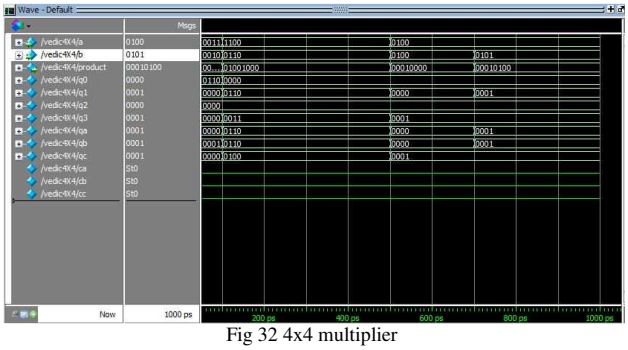


Fig 32 4x4 multiplier

7. CONCLUSION

This project proposed reversible sequential circuits based on conservative logic that is testable for any unidirectional stuck-at faults using only two test vectors, all 0s and all1s. The proposed sequential circuits based on conservative logic gates outperform the sequential circuit implemented in classical gates in terms of testability. The sequential circuits implemented using conventional classic gates do not provide inherited support for testability. Hence, a conventional sequential circuit needs modification in the original circuitry to provide the testing capability. Also as the complexity of a sequential circuit increases the number of test vector required to test the sequential circuit also increases. For example, to test a complex sequential circuit thousand of test vectors are required to test all stuck-at-faults, while if the same sequential circuit is build using proposed reversible sequential building blocks it can be tested by only two test vectors, all 0s and all 1s.

Thus, the main advantage of the proposed conservative reversible sequential circuits compared to the conventional sequential circuit is the need of only two test vectors to test any sequential circuit irrespective of its complexity. The reduction in number of test vectors minimizes the overhead of test time for a reversible sequential circuit. The proposed work has the limitation that it cannot detect multiple stuck-at-faults as well as multiple missing/additional cell defects. In conclusion, this paper advances the state-of-the-art by minimizing the number of test vectors needed to detect stuck-at-faults as well as single missing/additional cell defects.

REFERENCES

[1]. P. K. Saha, A. Banerjee, and A. Dandapat, "High Speed Low Power Complex Multiplier Design Using Parallel Adders and Subtractors," International Journal on Electronic and Electrical Engineering, (/JEEE), vol 07, no. II, pp 38-46, Dec. 2009.
[2]. R. E. Blahut, Fast Algorithms for Digital Signal Processing, Reading, MA: Addison-Wesley, 1987.
[3]. S. He, and M. Torkelson, "A pipelined bit-serial complex multiplier using distributed arithmetic," in proceedings IEEE International Symposium on Circuits and Systems, Seattle, W A, April 30-May-03, 1995,pp. 2313-2316.
[4]. J. E. VoIder, "The CORDIC trigonometric computing technique," IRE Trans. Electron. Comput., vol. EC-8, pp. 330-334, Sept. 1959.
[5]. R. Krishnan, G. A. Jullien, and W. C. Miller, "Complex digital signal processing using quadratic residue number systems," IEEE Trans. Acoust., Speech, Signal Processing, vol. 34, Feb. 1985.
[6]. T. Aoki, K. Hoshi, and T. Higuchi, "Redundant complex arithmetic and its application to complex multiplier design," in Proceedings 29th IEEE International symposium on Multiple-Valued-Logic, Freiburg, May 20-22,1999, pp. 200-207.
[7]. Z. Huang, and M. D. Ercegovac, "High-Performance Low-Power Leftto- Right Array Multiplier Design," IEEE Transactions on Computers, vol 54, no. 3, pp 272-283, March 2005.
[8]. S. Y. Kung, H. J. Whitehouse, and T. Kailath, VLSI and Modern Signal Processing, Englewood Cliffs, NJ: Prentice-Hall, 1985.
[9]. [9] P. Mehta, and D. Gawali, "Conventional versus Vedic mathematical method for Hardware implementation of a multiplier," in Proceedings IEEE International Cotiference on Advances in Computing, Control, and Telecommunication Technologies, Trivandrum, Kerala, Dec. 28-29,2009, pp. 640-642.
[10]. H. D. Tiwari, G. Gankhuyag, C. M. Kim, and Y. B. Cho, "Multiplier design based on ancient Indian Vedic Mathematics," in Proceedings IEEE International SoC Design Cotiference, Busan, Nov. 24-25, 2008, pp. 65-68.
[11]. J. S. S. B. K. T. Maharaja, Vedic mathematiCS, Delhi: Motilal Banarsidass Publishers Pvt Ltd, 200 I.
[12]. C. S. Wallace, "A suggestion for a fast multiplier," lEEE Trans. Electronic Comput., vol. EC-\3, pp. 14-17, Dec. 1964.
[13]. P. K. Saha, A. Banerjee, and A. Dandapat, "High Speed Low Power Factorial Design in 22nm Technology," in Proceedings AlP International Cotiference on Nanomaterials and Nanotechnology,