International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 2, Issue 11, November 2015)

A High Performance Dual Mode Logic Gate Design using Tanner Tool

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***Abstract*: Low power technology was major thought in gift generation circuits. so as to realize low power Sub-threshold circuit style is one in every of the leading ways for low power to ultra-low power applications. the twin Mode logic gates square measure designed to control within the sub threshold region. during this paper we have a tendency to discuss concerning dual mode logic gates with that we have a tendency to designed completely different forms of design of dual mode logic. These circuits square measure designed and that they square measure simulated with the Tanner Tools13.0 with TSMC018 Technology**

1. INTRODUCTION

In the gift generation, the key issues of the VLSI designer was the facility thought were space, performance, price and1. responsibility was principally became secondary importance. In gift years, however, this has begun to alter and, power is being given comparable weight to space and speed issues. many factors have obtained to the present trend. Infect the first driving issue has been the outstanding success and growth of the category of transportable devices (desktops, audio- video• devices) and wireless communications systems (personal• digital assistants and private communicators) that demand• high-speed computation and sophisticated practicality with• low power consumption.

2. SOURCES OF POWER DISSIPATION:

Power Dissipation majorly happens as a result of the 2 factors known as dynamic losses and static losses, These dynamic losses ar occurred as a result of the increasing in operation frequency of the devices. These losses occur as a result of shift activity of the transistors. Static losses not rely upon the frequency of operation it depends on the technology with that the scaling of transistors ar designed with high scaling issue has high static losses.

In order to control the circuit at low power consumption sub threshold plays a serious role. Circuits that operate within the sub-threshold region use a provide voltage that's near or but the brink voltages of the transistors, so there's a big reduction in each dynamic and static power consumption. The low-power twin mode logic (DML) family may be a logic family designed to control within the sub-threshold region. The planned logic family are often switched between static and dynamic modes of operation in line with system necessities. the power of DML circuits to control in each the static and dynamic modes provides the chance to make economical logic circuits that balance power consumption and in operation frequency (speed of the circuit) necessities. within the static mode of operation, the twin mode logic gates has terribly low-power dissipation with moderate performance, and within the dynamic mode of operation they need higher performance, at the worth of enhanced power dissipation.

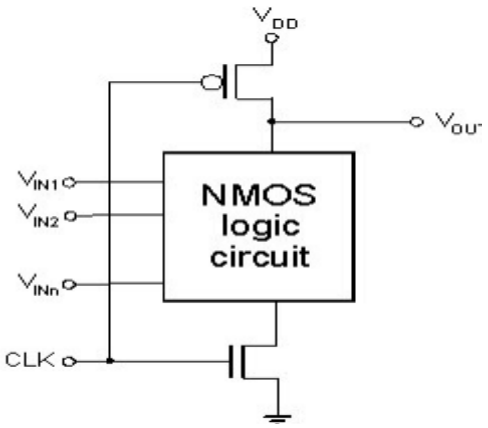
3. EXISTING LOGIC FAMILIES:

CMOS Logic Family: convention CMOS circuits are designed with a pull up network which will be formed by the PMOS and Pull down network will be formed by NMOS. It occupies 2N transistors for N inputs.

Key Features:

Rail to Rail swing
No steady state path between VDD and GND
Very robust under Process Variations
large capacitance Delay is function of load capacitance and transistor resistance
Very robust even in sub/near threshold regions

4. DYNAMIC LOGIC GATES:



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Unlike the CMOS structure Dynamic CMOS consists of only NMOS logic circuit was connected the VDD and GND are connected to NMOS logic by using PMOS and NMOS whose inputs are given to a clock signal. We can reduce the area of the circuit because of for N inputs we require only N+2 gates.
Here the dynamic gates are operated in two modes of operation dynamic and static mode
When CLK=0: PMOS will be in the ON state and the NMOS logic is in the OFF state, so the output was pre-charged to the VDD irrespective of inputs
When CLK=1: NMOS will be in ON state and PMOS will be in the Off state, so the evaluation of inputs are starts either main the pre-charged data or to discharge the data

Features:

- Very low static power dissipation.
- High noise margins (full rail to rail swing).
- Low output impedance, high input impedance
- No steady state path between VDD and GND.
- Delay is function of load capacitance and transistor resistance.
- Comparable rise and fall times (under the appropriate
- transistor sizing conditions)
- Very fast
- Increased power dissipation
- Charge Sharing, glitches
- Very high sensitivity to Process Variations

5. DUAL MODE LOGIC GATES:

These approaches utilize low supply voltages for digital circuit operation, decreasing the dynamic power quadratically and sufficiently reducing leakage currents; albeit, at the expense of loss in performance. The DML family, which is fully compatible with any standard logic process, was demonstrated to be fully functional at all operational regions, and up to nominal supply voltages.
The basic DML emerges from the both static and dynamic logic gates. DML gets acts as both as static gates and as dynamic gates. An additional footer /header transistor (connected in series to an evaluation path) is optional to ensure a correct interface with other gates.

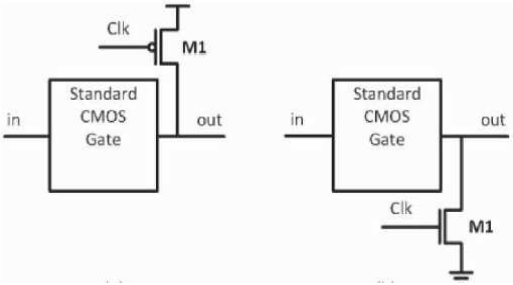

Fig.A: Type- A and Type –B of DML Logics

The Clk is feeded with an asymmetric clock, in dynamic mode operation, clk allows two distinct operations one dynamic phase and static phase The output is charged to high/low, Based on the DML topology of the gate, the output is charged to high/low throughout the pre charge phase. The output is analyzed and evaluated based on the values obtained at the gate inputs during evaluation phase of operation.
Here we shows two DML topologies Tpe A and Type B logics as shown in above figure

Type A is characterized by an addition of p-MOS transistor connected to output and the VDD, on pre charge phase, the PMOS will be in ON state and pre charges the output to a logical “1”
Implementation of dynamic logic gates makes use of a footer, which needs an extra transistor than the DML gates. During the evolution phase i.e clk=1 it acts like normal static CMOS gate.

DML gate was designed by adding extra semiconductor to output and therefore the ground throughout the pre-charge clinical test.e clk=1 the output was pre-chaged to the logic “0” and through the evolution part clk= zero its acts like traditional static gate.

DML nodes that operate in dynamic mode possess several deserves over ancient dynamic nodes that inheritable from DML topology. it's distinct potential to shift between varied operations modes. The DML genetically characterizes an energetic keeper made up of the CMOS complementary logic. it's nonheritable from the node structure that consists of totally purposeful CMOS half, and additionally supports in holding the output level. This very important constraint to the immunity to temperature fluctuations, method variations and breakdown domino’s fashionable disadvantages like disturbance noise, charge sharing and condition to glitches, that escalates with voltage and method scaling.

While planning a DML gate, the planning methodology used is to repair the pre charge semiconductor in parallel to the stacked transistors. As a result, analysis is finished supported the parallel transistors therefore makes it quicker. The stacked transistors are aligned to terribly low widths thus on cut back intrinsic capacitances, increasing dynamic operation performance over ablated static operation performance. This principle additionally reduces power dissipation in comparison to standard CMOS gates. The pre charge semiconductor is additionally unbroken at minimum size thus on cut back leak currents throughout analysis and static operation

All gates may be designed either as blood group or group B, neglecting the higher than mentioned optimisation tips. the best style methodology whereas planning with DML gates is to cascade connects blood group and kind B gates, specifically like in np-CMOS gates. this kind of style methodology is characterised by minimize space , most performance and most power potency, it's doable to attach same sorts of gates by creating use of associate degree electrical converter buffering

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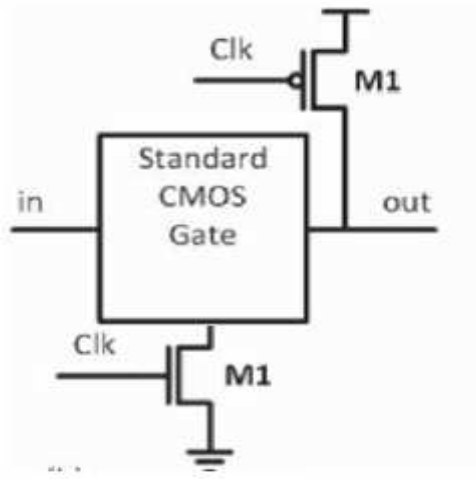
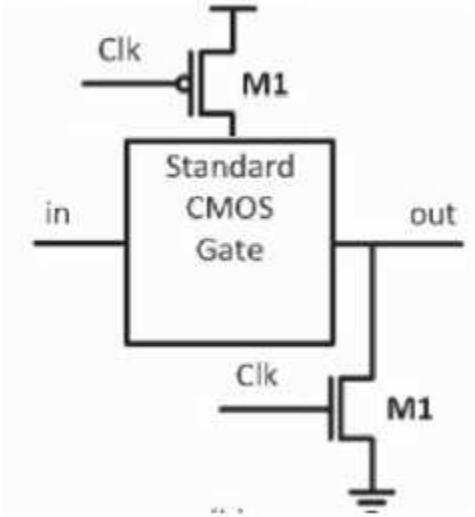
between them, as worn out the twin mode logic. Same sorts of gates may be connected while not inverters once a footer/header is employed at every stage, however, this technique ends up in glitching once pre charge ends and till the analysis information ripples through the chain. These square measure basic common challenges once planning with dynamic gates [11]. in comparison to the quality dynamic logic, DML's inherent keeper permits sick the logical worth

In this we show another two DML logic gates called Footed A and Footed B



Footed A is similar to the Type A logic design but here we adds a additional NMOS transistor in series to the NMOS logic. NMOS logic was grounded by using this additional nmos with clk signal. During Pre-charge phase PMOS will be in the ON state and pre-charges the output node at the same time NMOS will be in OFF state which will disconnects the ground from circuit in-order to reduce the static loss in pre-charge node.



Footed B is similar to the Type B logic design but here we adds a additional PMOS transistor in series to the PMOS logic. PMOS logic was connected to VDD by using this additional PMOS with clk signal. During Pre-charge phase NMOS will be in the ON state and pre-charges the output node at the same time PMOS will be in OFF state which will disconnects the VDD from circuit in-order to reduce the static loss in pre-charge node.

6. SIMULATION AND RESULTS:

These circuits are designed and simulated using the Tanner Tools.
The DML logic style are applied on the nor gate and therir power diispatins are hown below table

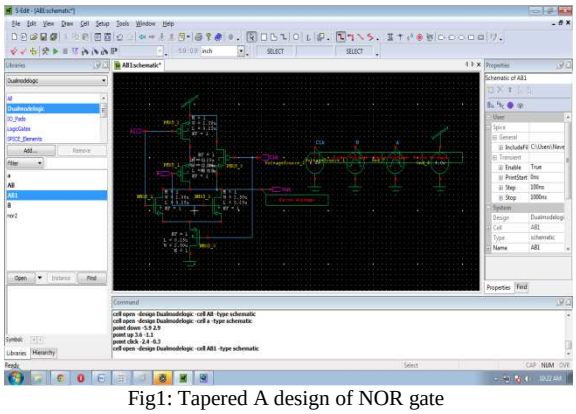


Fig1: Tapered A design of NOR gate

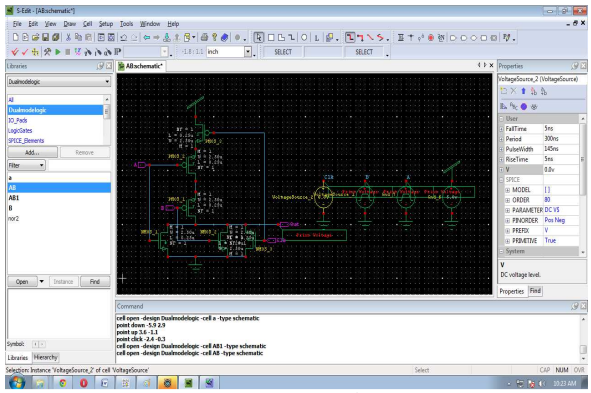


Fig2: tapered B design of NOR gate

Conclusion:
The novel Dual Mode Logic (DML) family of logic gates was considered as an energy efficient alternative to standard CMOS logic. On the fly tradeoff between High performance of dynamic mode and energy efficiency of static mode is enabled using DML and its following design methodologies. We can switch between these operation modes in real time by making use of DML methodology from the scope of a single gate and up to a complete design block.

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