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An Ultra Low Leakage High Performance Flipped Voltage Follower Design

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Abstract: ***Static power consumption has became a serious problem as we tend to area unit moving towards finer technologies. Power consumption is one amongst the highest considerations of VLSI circuit style, for which CMOS is that the primary technology. In bulk CMOS technology the body/substrate terminal of MOS transistor can be used as the fourth terminal. By applying a bias voltage (V SB) at this fourth terminal, V T can be modulated electronically due to the body effect. Body effect enables a variety of effective body biasing techniques. Body biasing is a key enabler of low-power circuit operation and has the potential to enhance the performance of a low voltage analog circuit. A MOS transistor with dynamic body bias technique is known as dynamic threshold MOS (DTMOS) transistor. In paper we Implement Fluffed Voltage Follower was designed using Tanner EDA.***

1. INTRODUCTION

Out surrounding world is analog in nature. Digital systems require analog to digital conversion at the front of the system and digital to analog conversion at its end. Analog computation and signal processing makes it simpler and faster [2]. Analog signal processing represents the signals as physical quantities like e.g. charge, current, voltage or frequency. These signals are continuous in value and continuous in time. Analog signal processing is most effective when precision is not the major criteria and when massive parallel collective processing of large number of signals that are continuous in time and amplitude is required [3]. In this thesis, we discuss the low voltage analog circuit design. The new smaller size process technologies offer opportunities to operate at higher frequencies consuming less power. For analog circuits, this fact partially applies since it is often the case that additional current is needed to keep the same performance when the power supply voltage is decreased Furthermoren ,for sub-micron technology It would not be possible to use voltage doublers to enhance the circuit performance due to low breakdown voltage of the transistors [4]

Driven by low-power and low-voltage requirements for integrated mixed-signal portable applications, analog signal processing circuits such as four-quadrant analog multipliers are becoming more compact and operate with lower supply voltages. Concentrating on circuit topologies, a circuit cell called "flipped voltage follower" (FVF) has been popularly used for low-voltage design since it needs only a supply voltage of $V_{TH} \square V_{eff}$, where V_{TH} is the threshold voltage and V_{eff} $(=V_{GS} - V_{TH})$ is the effective gate voltage.

2. THE FLIPPED VOLTAGE FOLLOWER

2.1. Source follower

The source follower (common-drain configuration) is shown in Figure 3.1(a). The input signal is applied to the gate and the output is taken from the source. From a large-signal standpoint, the output voltage is equal to the input voltage minus the gate-source voltage. The gate-source voltage consists of two parts: the threshold voltage and the overdrive voltage. If both parts are constant, the resulting output voltage is simply offset from the input, and the small-signal gain would be unity. Therefore, the source follows the gate, and the circuit is also known as a s*ource follower*. In practice, the body effect changes the threshold voltage, and the overdrive depends on the drain current, which changes as the output voltage changes unless $R_L \rightarrow \infty$. Furthermore, even if the current were exactly constant, the overdrive depends to some extent on the drain-source voltage unless the Early voltage is infinite.

2.2 Flipped voltage follower cell

Let us consider the common drain amplifier in Figure commonly used as a voltage buffer. This circuit is also known as a "source follower". If body effect is neglected the circuit follows the input voltage with a dc level shift, i.e. $V_o \square V_i - V_{SG1}$. Where V_{SG1} is the source-to-gate voltage of transistor M_1 . Concerning the large-signal behavior, this circuit is able to sink a large current from the load, but it sourcing capability is limited by the biasing current source I_b . A drawback of this circuit is that current through transistor M_1 depends on the output current, so that V_{SG1} is not constant and, hence, for resistive loads, the small and large signal voltage gains are less than unity

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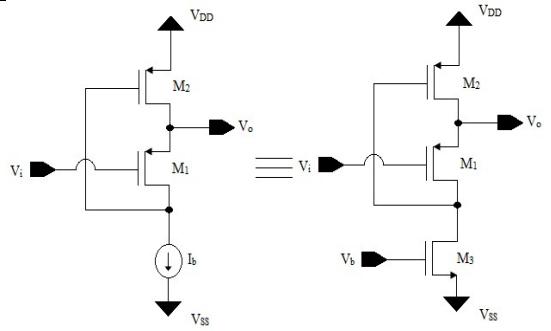


Fig1: Flipped voltage follower cell.

The circuit in Fig 1 is another source follower where the current through transistor M1 kept constant independent on output current. It could be described as a follower with shunt feedback. Neglecting the short-channel effect, V_{SG1} is held constant,

and voltage gains are unity. Unlike the conventional voltage follower, the circuit in Figure 3.3 is able to source a large amount of current, but its sinking capability is limited by the biasing current source I_b, the large sourcing capability is due to the low impedance at the output node ($r_1 g_{m1} g_{m2} r_1$), where g_{mi} and $_{oi}$ are the trans- conductance and output resistance, respectively. This value is in the order of 20-100.

3. DTCMOS

In addition, analysis and development on high potency is crucial to maximise the utilization of moveable device that are most popular numerous functions than within the past. PMIC for prime potency sometimes amendment drastically from linear regulator to switch regulator. however the switch regulator have disadvantage of low potency compared with linear regulator at lightweight load conditions. Therefore, this paper is bestowed the mistreatment of switch regulator at significant load conditions. All power offer device of Mobile appliance should be created stable and numerous DC output voltage of high effectiveness from a unstable DC input power offer.. For that reason, it's used do an influence offer of Switched Mode Power offer(SMPS) methodology rather than an influence offer of typical linear methodology. Therefore, during this paper, the facility provides are designed mistreatment DT-CMOS that is low on resistance than CMOS Switching loss is fixed cause, but conduction loss by on resistance of switch is increased by a output current increased. When output current is increased, conduction loss is increased more than switching loss in high output current. Finally, switch development that have low on-resistance to heighten efficiency of SMPS is essential. In this paper, we proposed available DT-CMOS without high leakage currents in high power supply voltages using this DT-CMOS's concept. The proposed DT-CMOS in this paper can be seen in Fig. 3. When the switch is became ON, the body voltage of the switch MOS is controlled by diode connection CMOS and the threshold voltage is lowered. When the switch is became OFF, body of CMOS is connected to each the power supply and the ground..

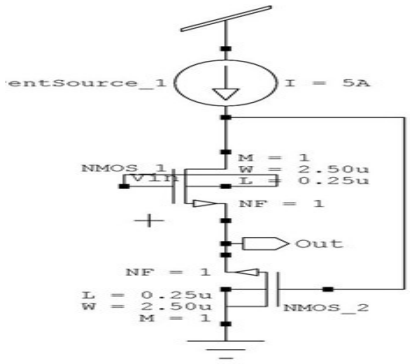
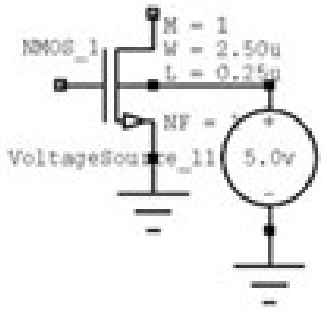


Fig2: DTCMOS Flipped Voltage Follower

Variable body biasing technique:
This is another new leakage reduction technique, which we call the ''Variable body biasing'' technique

Self Bias:



If we are connecting a additional substrate voltage to transistor it can be acts like a high threshold transistor so that we can minimize the leakage in it.

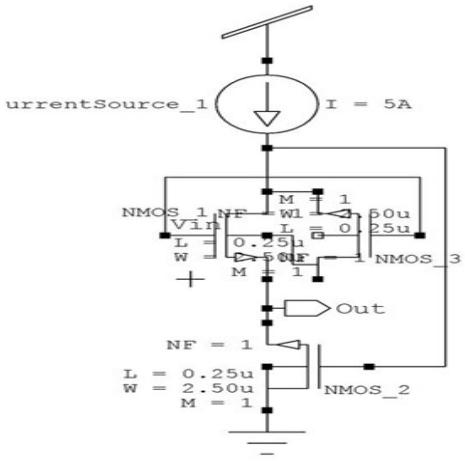


Fig3: Variable body biasing Flipped Voltage Follower

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4. SIMULATION

This circuits are designed using S-Edit and Simulated using Tanner T-Spice using TSMC018 Technology.

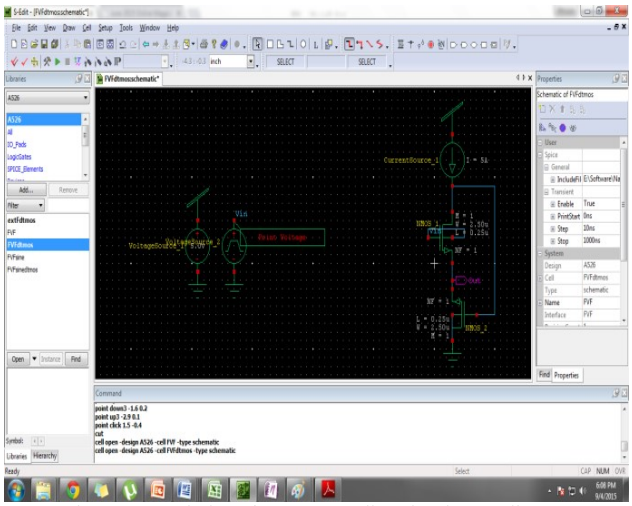

Fig4: S-EDIT design of DTCMOS Flipped Voltage Follower

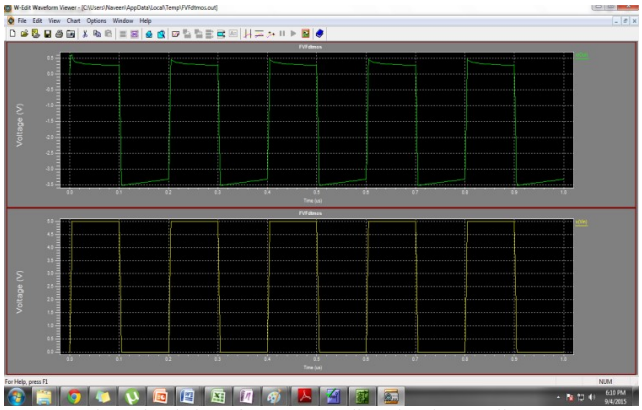

Fig5: Simulation of DTCMOS Flipped Voltage Follower

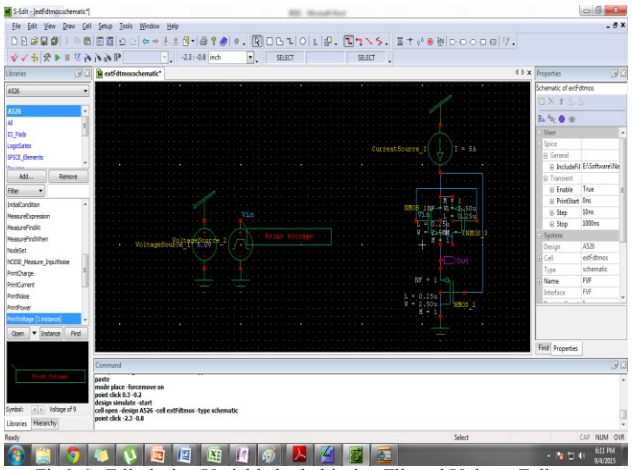

Fig6: S- Edit design Variable body biasing Flipped Voltage Follower

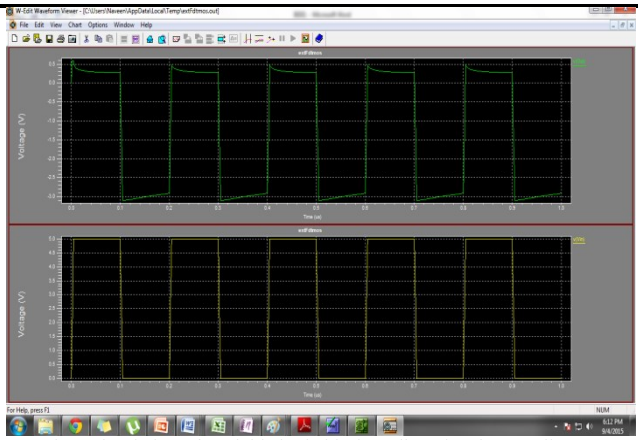

Fig7: Simulation of Variable body biasing Flipped Voltage Follower

CONCLUSION

In this paper, body effect present in conventional FVF topology has been utilized positively using DTMOS transistor The proposed FVF outperforms the conventional FVF in terms of more symmetrical slew-rate and increased output signal range for which FVF is able to follow input linearly. It is pertinent to mention that these improvements are achieved for same bias current and size of MOS transistor without requiring any additional devices. The important feature of DTMOS is that no extra circuitry is required for body bias voltage generation, as in other body bias techniques. DTMOS approach virtually has no effects on the overall silicon area of proposed FVF and is compatible with standard bulk CMOS process.

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