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Step up Converter Design using Body Bias Technique

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Abstract: **CMOS is used to construct the integrated circuits with low level of static leakage. With this low level leakage we are designing all the transistor circuits in CMOS logic. To control this static leakage in the circuits the supply voltage is a major concern. Here the step-up converters with charge pump and the level for maintaining its threshold voltage (V_T) is to be analyzed and proposed. Here we are going to propose the novel approach as body bias effect and sub-threshold logic. This will be applied for the step-up converters for energy harvesting applications. In this paper we design a step up converter using Variable body bias technique using Tanner EDA Tools.**

Keywords: **CMOS, Step-Up Converter, Body-bias**

1. INTRODUCTION

CHARGE PUMP:

A charge pump circuit provides a voltage that is higher than the voltage of the power supply or a voltage of reverse polarity. In many applications such as Power IC, continuous time filters, and EEPROM, voltages higher than the power supplies are frequently required. Increased voltage levels are obtained in a charge pump as a result of transferring charges to a capacitive load and do not involve amplifiers or transformers. For that reason a charge pump is a device of choice in semiconductor technology where normal range of operating voltages is limited. Charge pumps usually operate at high frequency level in order to increase their output power within a reasonable size of total capacitance used for charge transfer. This operating frequency may be adjusted by compensating for changes in the power requirements and saving the energy delivered to the charge pump.

Among many approaches to the charge pump design, the switched-capacitor circuits such as Dickson charge pump are very popular, because they can be implemented on the same chip together with other components of an integrated system. The voltage gain of Dickson charge pump is proportional to the number of stages in the pump. It may cost quite many devices and silicon area, when a charge pump with the voltage gain larger than 10 or 20 is needed. Such high voltage gains are required for low voltage EEPROMs, and typically more than three stages of Dickson charge pump are used. Improved Dickson charge pumps for low voltage EEPROMs and flash memories are developed. Charge pump operates by switching ON and OFF a large number of MOS switches which charge and discharge a large number of capacitances, transferring energy to the output load. Large amount of energy is lost whenever the load current is reduced. Savings of switching energy were primary reason for the design efforts, where a special circuit organization was proposed to regulate switching frequency whenever a requirement for the load current changes. There is a need for better understanding of the design tradeoffs related to charge pump design.

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Among many approaches to the charge pump design, the switched-capacitor circuits such as Dickson charge pump are very popular, because they can be implemented on the same chip together with other components of an integrated system. Many research works focused on the design and timing scheme of Dickson charge pump had been accomplished such as high. Witters et al. provided a detailed analysis of Dickson multiplier built in VLSI technology with diodes realized by nMOS transistors. They considered effects of threshold voltage and leakage current as well as conducted a number of experimental measurements.

Charge pump operates by switching on and off a large number of MOS switches which charge and discharge a large number of capacitances, transferring energy to the output load. Large amount of energy is lost whenever the load current is reduced. Savings of switching energy were primary reason for the design efforts presented, where a special circuit organization was proposed to regulate switching frequency whenever a requirement for the load current changes. In addition, simulation and measurement results presented in indicated a strong dependence of the output voltage on the

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load resistance. There is a need for better understanding of the design tradeoffs related to charge pump design.

3.

By constructing a network which reaches this upper limit, we can demonstrate that the limit is an attainable upper bound. An example organization of the multiphase charge pump with the voltage gain equal to the upper bound is shown in Fig. This circuit includes 4 switches per a single capacitor; therefore it exceeds the upper limit on a number of switches per capacitor for a two phase voltage multiplier that was estimated in as not more than 3-2/n. In addition, the maximum gain structure requires non-overlapping clocks of different frequencies to control these switches. However, MOS switches designed in the charge pumps use much smaller area than capacitors and are not detrimental for the pump performance.

A charge pump is a three position electronic switch which is controlled by the three states of PFD. When switch is set in UP or DOWN position, it delivers a pump voltage $\pm VP$ or a pump current $\pm IP$ to the loop filter. When both UP and DOWN of PFD are off, i.e. N position, the switch is open, thus isolating the loop filter from the charge pump and PFD. Figure shows the basic charge pump.

The inherent mismatches between these two switches results in mismatch in charging and discharging current in addition to timing mismatch. Hence there is variation in control voltage at the output. In fact the W/L ratios are adjusted so as to have equal UP and DOWN currents. Even though, about 73µA mismatching is observed between these currents in simulation. That means, since two current sources are themselves mismatched, the control voltage experiences the random changes in it.

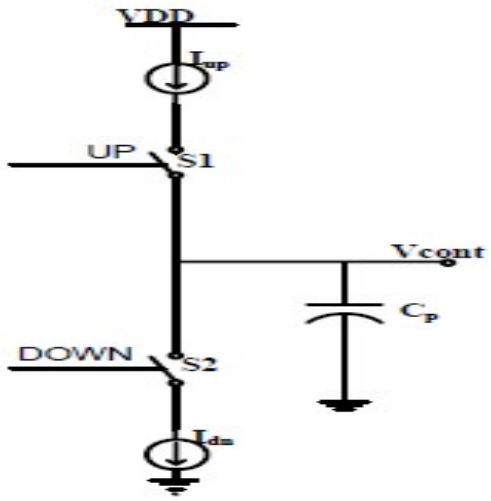

Fig 1. Basic Charge Pump Architecture.

2. DICKSON CHARGE PUMP

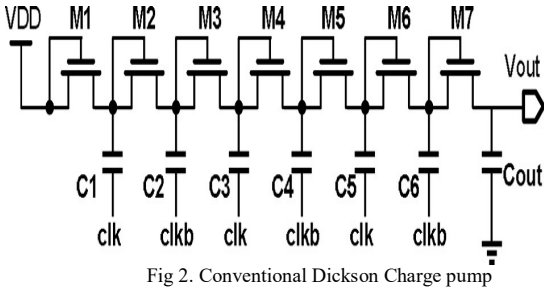

Fig 2. Conventional Dickson Charge pump

The Dickson charge pump and single cascade charge pump, shown in fig. , are derived from the ideal diode charge pump architecture. Both circuits output voltage obey equation that can be simplified as in equation.

$$Vout = VDD - Vth(0) + \Sigma [\alpha VDD - Vth(i)] \quad (1)$$

$$Vout = VDD + n (VDD\text{-}Vth) \quad (2)$$

The term VDD-Vth is called the voltage gain per unit stage. Note that this gain is additive and not multiplicative as in the voltage doubler architecture. In the Dickson charge pump, as the voltage of each stage increases, the threshold voltage of the diode-connected MOSFET increases due to body effect, and the voltage gain decreases as the number of stages increases. This effect is not present with the single cascade architecture. For large number of stages (>10), the Dickson charge pump has an average voltage gain of 0.25*VDD, while the single cascade circuit produces an average gain of 0.5*VDD.

In Wu Chang charge pump circuit the substantial uses of the circuit does not mismatch the p-MOS and the n-MOS conditions of the stages. And also this stage requires the more loop filters and also more current sources. Then this stage of the circuit occupies large silicon area of the chip causes more noises. Then charge pump circuit having the clock feed through and also this is not fully eliminating the charge sharing problems.

The Linear charge pump circuit having the limiting output voltage level form the desired area of the circuit conversion from the number of stages. This inverter level coupling stages could be providing amplitude degradation. And also providing switch mismatch condition for the all dead zone. By using this single ended coupling from the stages of all the coupling inverter gives the results for the more number of parasitic capacitance

3. PROPOSED SYSTEM

The proposed charge pump has the six stages and then the coupling of the inverter stages and also for each branch. The body biasing and the backward control scheme has been applied to the each number of coupling stages and also could be provide the node level of separation from the each stages. The inverter coupling could be processed under the technology that could be beyond the network based applications.

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The each node of operation having the reverse biasing voltages and also could be processed for the more stages form the applications. The proposed charge pump has been used for the real time implementation of the Phase Locked Loop. This is the feedback combining system for the linear process that could be connected to the phase detector and the voltage controlled oscillator for the process of all variations from the units. This could be fixed the low frequency signal for the extension of the phase variations from the two input signals

The proposed charge pump circuit has been shown in Fig 2. The stages of inverter coupling have been adopted from the four level of inverter. This could be connected to the each branch of the circuits for the linear operation of the six stages of the proposed charge pump. The inverter coupling and also the capacitance (1pF) of the 1st stage of the two branches has been given to the input voltage supply.

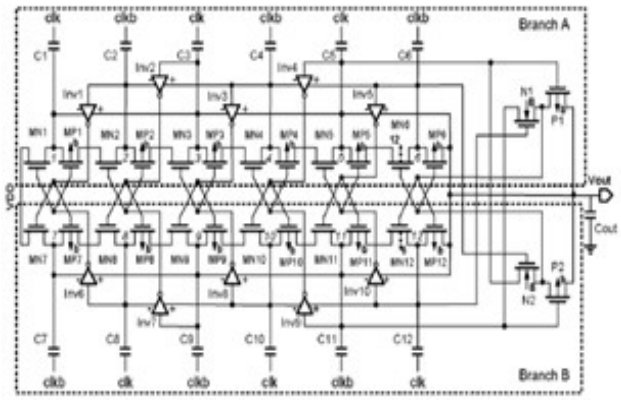

Fig 3

The capacitors from c1 to c6 in the two branches are used for the charging and discharging of the energy consumption based technique and also used for the amplification of the input voltage from the each stages. Then the body biasing can be applied from the node 1 of the c1 and the MN1 coupling with the MP1. This could be transferred to the branch B of the capacitance node 7 of c1. The coupling of the MN7 and the MP7 (Fig 4) of branch B gives the amplitude stage of first level voltage from the capacitor. The clock frequency has to be given into the circuit combination from the clk and clkb to the two branches.

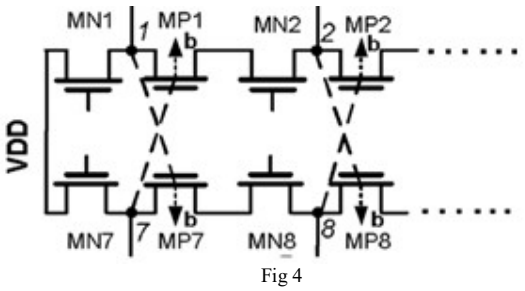

Fig 4

The clock supply and the input voltage (in milli volts) given to the first coupling of the inverter stage and then the body biasing node could be activated from the MN1 to MP7 and following to the all stages from the n-MOS to p-MOS. The second stage i.e the backward control and the reverse coupling of the MN2 from MN8 and also the MP2 from MP8. Then this node of operation can be better and improves when compared to the first node of operation. Then for the each level of stages can be amplified as per the backward control and the biasing node through the channel operation from the each number of stages

This could be coupling and does not carry any dead zone of operation and this could be switching to the prominent to the all stages. The capacitance from the c1 of each branch carries the unit supply of the voltage from clk to clkb. Then the last stage from the n-MOS N1 and this could be coupling with the N2 and then the P1 coupling with the P2 having the amplitude switching. Then this storage from the each stages of the coupling from the node of operation can also to be calculated from the structural of the node 1 to 8. Then another node of bulk connection has been applied from the N1 to the P1 of linear stages. This could be effectively reduces the parasitic capacitance from the charge pump

This proposed charge pump has advantages of the low power consumption based on body biasing bulk connection from the each node of operation. And also this charge pump circuit has been enabled for the lower input voltage (in milli volts) having the bulk output voltages from the clock pulses. The enabling signals that carry the circuit level of operation from the amplitude degradation of the unit supply to the needed positive up gradation from the input amplitude. This phase difference from the clock pulses into the bulk connection from the unit supply that can be varied as per the input signal

The required connection between these signals has been proposed and implemented into the phase locked loop. This could be having the phase detector, Charge pump and the voltage controlled oscillator. The level of connection is to be a feedback signal from the VCO to the input voltage. The phase difference from the input and the feedback signals has been applied to the phase detector. Then the charge pump gives the amplification of the input voltage from the phase detector. The variations of the phase frequency has been identified and also applied for the frequency synthesizer

4. SIMULATION RESULTS

The existing Dickson charge pump circuit and the are shown. The designing of this charge pump are designed in TANNER EDA

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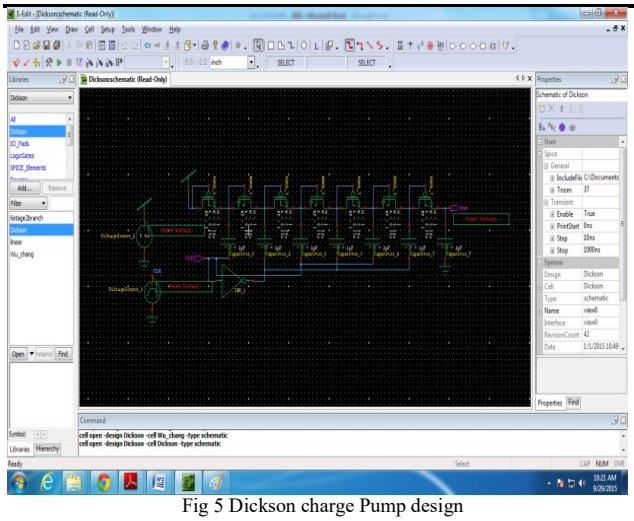

Fig 5 Dickson charge Pump design

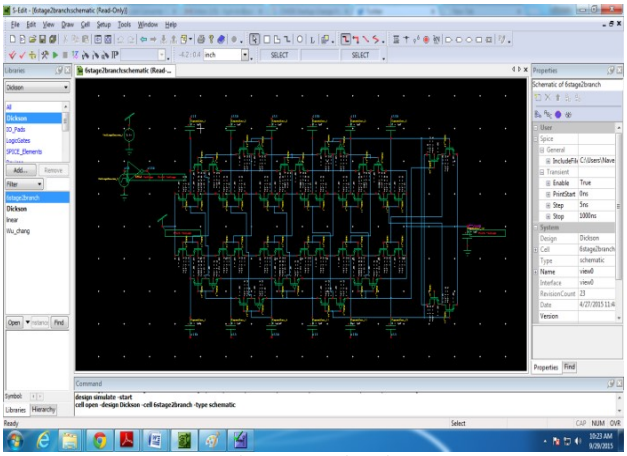

Fig 6 Proposed Design

These Circuits are simulated and their power consumption was tabulated was shown below table

Circuit	Power Consumption
Wu and Chang charge pump	5.197384e-003 watts
Linear Charge Pump	3.875069e-003 watts
Dickson Charge Pump	1.343997e-006 watts

CONCLUSION

Charge pump based on body biasing and the backward control scheme has been proposed in this system. The power and the amplification could be efficient when compared to the other existing charge pump. The low output ripple and high system stability of the dual-phase charge pump circuit are demonstrated by the test chip and get better performance. Therefore, the transient response and driving capability can be improved. Besides, only one closed-loop regulation is utilized to generate the charge pump circuit so as to improve the power conversion efficiency. By using this efficiency calculation the pumping efficiency also calculated and gets the detailed configuration of the proposed charge pump parameter evaluation. The degradation of the amplification could be highly reduces and it could be generated as per the test identification stages proposed in the charge pump design circuit. This circuit could be further used for the implementation of the like PLL based analog devices.

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