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An efficient Adiabatic Frequency Divider Circuit design using Tanner

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Abstract: Frequency dividers square measure crucial circuits that square measure utilized in PLLs and high-speed serialize/deserializers. The flip-flop-based frequency dividers square measure comprised of 2 D latches in cascade, and during a feedback configuration. The digital operation of this kind of dividers provides the advantage of suppressing the sensitivity to wave distortions. what is more, the flip-flop-based dividers bring home the bacon a good information measure than different kinds of frequency dividers at low-to-medium vary of frequencies. This paper presents a high-speed DFAL flip-flop-based frequency divider incorporating a brand new high-speed latch topology, that provides satisfactory performance for frequencies up to seventeen gigacycle per second. This circuit is meant and simulated during a customary 0.18µm CMOS method.

Keywords: Frequency Divider, D Latches, DFAL

I. INTRODUCTION

In the past few decades agone, the industry has been experiencing AN new spurt in growth, due to the employment of integrated circuits in computing, telecommunications and shopper natural philosophy. we've got come back an extended approach from the only semiconductor era in 1958 to the current day ULSI (Ultra Large Scale Integration) systems with quite fifty million The ever-growing range of semiconductors integrated on a chip and therefore the increasing transistor shift speed in recent decades has enabled nice performance improvement in pc systems by many orders of magnitude. sadly, such extraordinary performance enhancements are in the middle of a rise in power and energy dissipation of the systems. Higher power and energy dissipation in high performance systems need costlier packaging and cooling technologies, increase value, and reduce system responsibleness. even so, the extent of on-chip integration and clock frequency can still grow with increasing performance demands, and therefore the power and energy dissipation of superior systems are a crucial style constraint.

For example, high-end microprocessors in 2010 square measure expected to use billions of transistors at clock rates over 30GHz to realize TIPS (Tera directions per seconds) performance [1]. With this rate, high-end microprocessor's power dissipation is projected to succeed in thousands of Watts. This thesis investigates one in all the foremost sources of the power/energy dissipation and proposes and evaluates the techniques to cut back the dissipation.

Digital CMOS integrated circuits are the drive behind VLSI for top performance computing and different applications, associated with science and technology. The demand for digital CMOS integrated circuits can still increase within the close to future, thanks to its vital salient options like low power, reliable performance and enhancements within the process technology. In paper we designed a frequency divider circuit using DFAL Based latch design qith reduced dynamic power was explained in the below sextions

II. NEED FOR LOW POWER DISSIPATION CIRCUITS

DESIGN:

There square measure varied interpretations of the Moore's Law that predicts the expansion rate of integrated circuits. One estimate places the speed at 2X for each eighteen months. Others claim that the device density will increase ten-fold each seven years. notwithstanding the precise numbers, everybody agrees that the expansion rate is speedy with no signs of retardation down. New generations of process technology square measure being developed whereas gift generation devices square measure at terribly safe distance from the elemental physical limits. a desire for low power VLSI chips arises from such evolution forces of integrated circuits. The Intel 4004 chip, developed in 1971, had 2300 transistors, dissipated concerning one watts of power and clocked at one megacycle per second. Then comes the Pentium in 2001, with forty two million transistors, dissipating around sixty five watts of power and clocked at a pair of.

While the facility dissipation will increase linearly because the years blow over, the facility density will increase exponentially, owing to the ever-shrinking size of the integrated circuits. If this exponential rise within the power density were to extend ceaselessly, a chip designed some years later, would have identical power as that of the apparatus. Such high power density introduces responsibleness issues like, electromigration, thermal stresses and hot carrier evoked device degradation, leading to the loss of performance.

Another issue that fuels the requirement for low power chips is that the redoubled market demand for transportable shopper natural philosophy hopped-up by batteries. The looking for smaller, lighter and a lot of sturdy electronic merchandise

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indirectly interprets to low power necessities. Battery life is changing into a product somebody in several transportable systems. Being the heaviest and largest element in several transportable systems, batteries haven't skilled the similar speedy density growth compared to the electronic circuits. the most supply of power dissipation in these high performance battery-portable digital systems running on batteries like note-book computers, cellular phones and private digital assistants square measure gaining prominence. For these systems, low power consumption could be a prime concern, as a result of it directly affects the performance by having effects on battery longevity. during this scenario, low power VLSI style has assumed nice importance as an energetic and quickly developing field.

Another major demand for low power chips and systems comes from the environmental issues. trendy workplaces square measure currently equipped office automation equipments that consume great amount of power. A study by yankee Council for AN Energy-Efficient Economy calculable that workplace instrumentality account for five for the whole America business energy usage in 1997 and will rise to 100% by the year 2004 if no actions square measure taken to stop the trend

III. OVERVIEW OF POWER DISSIPATION OF CIRCUITS

t is a lot of convenient to speak concerning power dissipation of digital circuits at now. though power depends greatly on the circuit vogue, it may be divided, in general, into static and dynamic power. The static power is generated thanks to the DC bias current, as is that the case in transistor-transistor-logic (TTL), emitter-coupled logic (ECL), and N-type MOS (NMOS) logic families, or thanks to run currents. all told of the logic families aside from the push-pull sorts like CMOS, the static power tends to dominate. that's the rationale why CMOS is that the most fitted circuit vogue for terribly giant scale integration (VLSI).

CMOS is that the logic family most popular in several styles thanks to following reasons:-

(a) Impeccable noise margins.
(b) Perfect logic levels.
(c) Negligible static power dissipation.
(d) Gives sensible performance in most cases.
(e) Easy to induce a purposeful circuits.
(f) Lot of tools accessible to change the look method.

The power consumed once the CMOS circuit is in use may be rotten into 2 basic classes: static and dynamic

3.1STATIC POWER

The static or steady state power dissipation of a circuit is expressed by the following relation [1]

$$Pstat = IstatVDD$$

Where, Istat is that the current that flows through the circuit once there's no shift activity. Ideally, CMOS circuits dissipate no static (DC) power since within the steady state there's no direct path from VDD to ground as PMOS and NMOS transistors square measure ne'er on at the same time. Of course, this state of affairs will ne'er be realised in follow since essentially the MOS semiconductor isn't an ideal switch. Thus, there'll continually be run currents and substrate injection currents, which is able to provide to a static element of CMOS power dissipation.

3.2DYNAMIC POWER

The dynamic part of power dissipation arises from the transient change behavior of the CMOS device. At some purpose throughout the change transient, each the NMOS and PMOS devices are turned on. this happens for gate voltages between Vtn and VDD - Vtp . throughout now, a short-circuit exists between VDD and ground and therefore the currents square measure allowed to flow. an in depth analysis of this development by Veendrick reveals that with careful style of the transition edges, this part may be unbroken below 10-15% of the full power [2]; this may be achieved by keeping the increase and fall times of all the signals throughout the planning inside a set vary (preferably equal). Thus, though short dissipation cannot continuously be utterly unheeded, it's on no account the dominant part of power dissipation in well-designed CMOS circuits. Instead, dynamic dissipation because of capacitance charging consumes most of the ability.

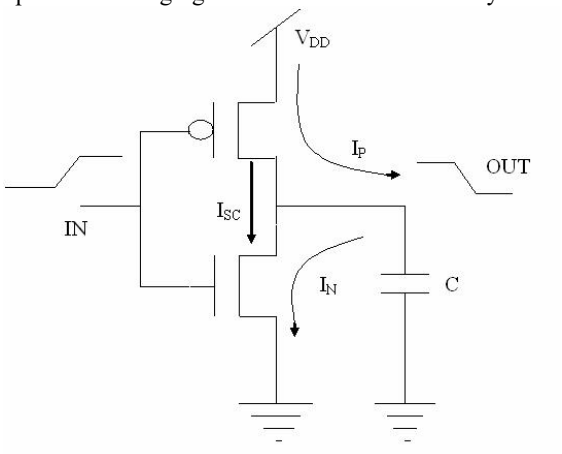

Fig1. CMOS Inverter for Power Analysis

So, to scale back the ability dissipation, the circuit designer will minimize the change event, decrease the node capacitance, cut back the voltage swing or apply a mixture of those strategies. Yet, all told these cases, the energy drawn from the ability provide is employed just one occasion before being dissipated. to extend the energy potency of the logic circuits, alternative measures may be introduced for usage the energy drawn from the ability provide.

A novel category of logic circuits known as adiabatic LOGIC

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offers chance|the likelihood|the chance} of more reducing the energy dissipated throughout the change events and therefore the possibility of usage or reusing a number of the energy drawn from the ability provide [3]. To accomplish this goal, the circuit topology and therefore the operative principle need to be changed, typically drastically. the quantity of energy usage possible victimization adiabatic techniques is additionally determined by the fabrication technology, change speed and therefore the voltage swing.

IV. DIODE FREE ADIABATIC LOGIC

shows the circuit diagram and simulated The schematic of DFAL resembles the static CMOS logic; but circuit operates in adiabatic manner. The nMOS semiconductor device (M3) within the pull down network adjacent to the M2
is used to exchange the diode for the discharging. Power clock (VPC) controls the turning ON and OFF of this semiconductor device (M3). the most power dissipation in reportable adiabatic circuits in their discharging path happens at the (MOS) diodes because of the edge fall (nonadiabatic loss) whereas in our planned circuit it's because of the ON resistance (adiabatic loss) of channel of MOS semiconductor device money supply. the ability dissipation because of this ON resistance (of M3) is considerably power than the ability dissipation because of the edge fall through diodes. conjointly money supply is employed to recycle charges from the output node thus the adiabatic losses may be recovered more. but the losses can not be utterly recovered and power dissipation can not be removed utterly as a result of the planned logic circuit is non reversible. thus by victimization MOS semiconductor device money supply, power dissipation is massively reduced compared to the diode primarily based adiabatic circuits

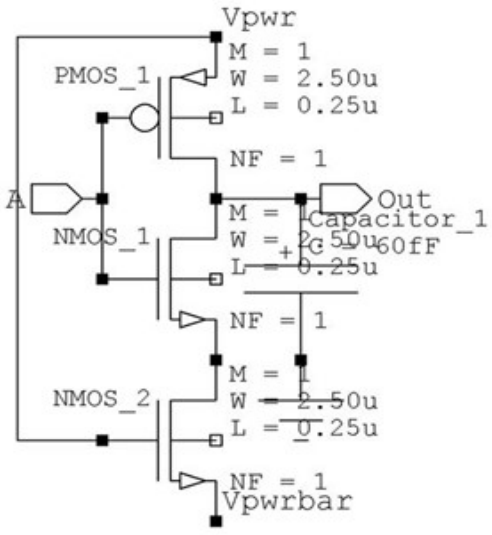

Fig2: DFAL Inverter Design

The schematic of DFAL resembles the static CMOS logic; but circuit operates in adiabatic manner. The nMOS semiconductor device (M3) within the pull down network adjacent to the M2
is used to exchange the diode for the discharging. Power clock (VPC) controls the turning ON and OFF of this semiconductor device (M3). the most power dissipation in reportable adiabatic circuits in their discharging path happens at the (MOS) diodes because of the edge fall (nonadiabatic loss) whereas in our planned circuit it's because of the ON resistance (adiabatic loss) of channel of MOS semiconductor device money supply. the ability dissipation because of this ON resistance (of M3) is considerably power than the ability dissipation because of the edge fall through diodes. conjointly money supply is employed to recycle charges from the output node thus the adiabatic losses may be recovered more. but the losses can not be utterly recovered and power dissipation can not be removed utterly as a result of the planned logic circuit is non reversible. thus by victimization MOS semiconductor device money supply, power dissipation is massively reduced compared to the diode primarily based adiabatic circuits

Circuit Operation. counting on the availability clock signal phases, circuit operation is split into 2 stages, analysis and hold. In analysis part VPC swings up whereas VPC swings down; but in hold part VPC swings down and VPC swings up as shown in Figure 1(b). In analysis part, once the output node is LOW and pMOS tree is turned ON, load capacitance CL is charged through pMOS semiconductor device (M1) leading to the HIGH state at the output. more once output node is HIGH and nMOS tree activates, discharging and usage of charges to the ability clock (VPC) via nMOS semiconductor device (M2 and M3) happens, leading to the output logic state to be LOW

In hold part, once output node is LOW and nMOS tree is ON, no transitions occur at the output. an equivalent method happens once the output node is HIGH and pMOS tree is ON. because of the hold part, dynamic change is reduced and so energy dissipation is additionally reduced.

This DFAL primarily based was applied to a Frequency divider circuit inorder to scale back the dynamic power within the Circuit.

A frequency divider, conjointly remarked as a clock divider, produces Associate in Nursing output whose frequency may be a fraction of the input frequency

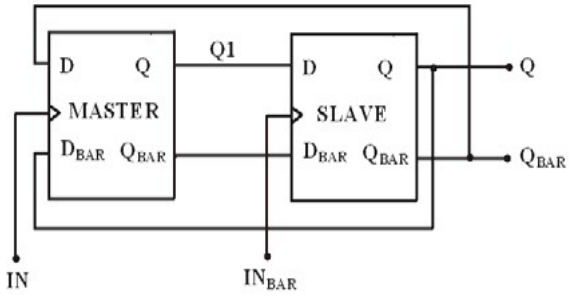

Fig3: Divide by 2 frequency divider using D Flip-Flop

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V. COUNTER VICTIMIZATION FREQUENCY DIVIDED BY TWO AND FOUR AND EIGHT VICTIMIZATION DFAL FREQUENCY DIVIDER

The counter consists of three stages of cascaded D Flip-flops. The D Flip-flop style has been enforced victimization DFAL and 2 D latch with one clock and one input. The clock input is applied to future flip flop comes from the output of its straight off preceding flip flop. For initial or instance the output of the primary register acts because the clock input to the second register and therefore the output of the second register feed the clock input of third register. The second register will turn solely when the output of initial register will modification its state.

that's the second incontrovertible fact that it gets its own clock input from output of the primary and not from the input clock. now delay here the add of propagation delay of 2 flip flops. therefore during this counter four register can turn solely when a delay adequate to fourfold the propagation delay of 1 flip-flop.

VI. SIMULATION

The DFAL based mostly divided by two frequency divider was designed victimisation S-EDIT and these simulations square measure dispensed in T-Spice victimisation TSMC018 Technology

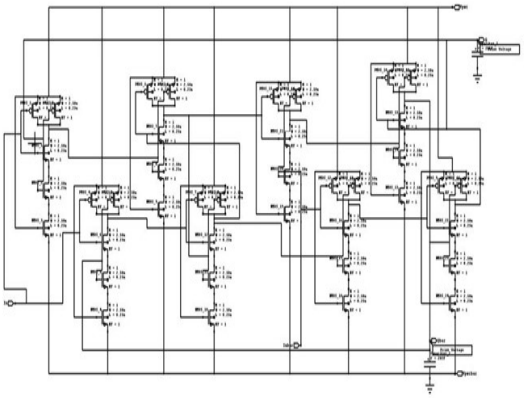

Fig4: Schematic design of Frequency Divider Circuit

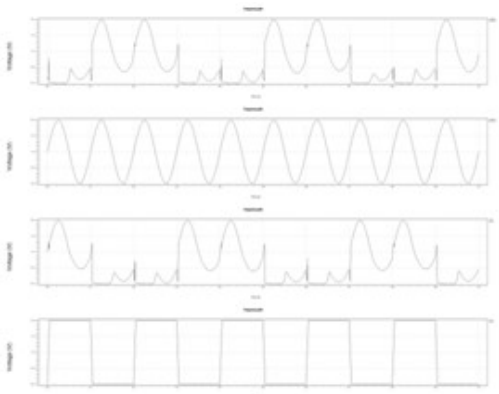

Fig5: Simulation of Frequency Divider Circuit

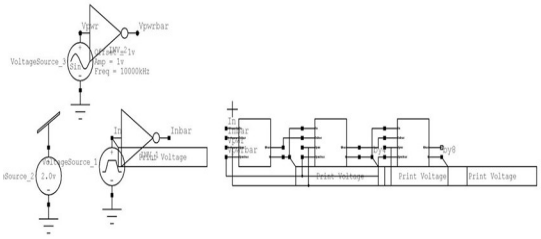

Fig6: Schematic design of frequency divided by 2 and 4 and 8

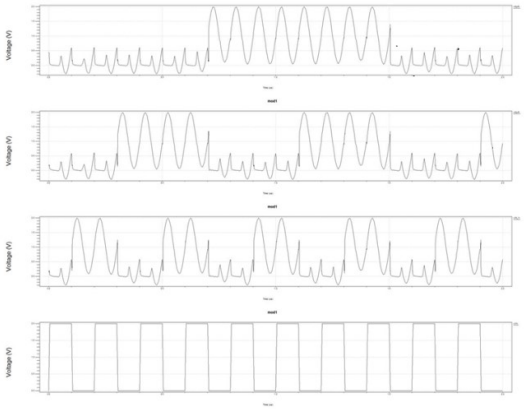

Fig7: Simulation of frequency divided by 2 and 4 and 8

Tabulation:

The below tabulation consists of Power Consumption of the frequency divider with different loads

For Inverter

Circuit	Power Dissipation
CMOS Inverter	2.077053e-005 watts
DFAL Based Inverter	6.728647e-007 watts

For Frequency Divider:

Circuit	Power Dissipation	Delay
Conventional FD	1.447677e-005 watts	1.5070e-007
2PSAL FD	2.701592e-006 watts	7.5266e-008
DFAL FD	2.039176e-006 watts	2.7182e-008

CONCLUSION

DFAL technique was the economical technique so as to cut back the dynamic losses within the flip-flop. This methodology was extended to use on the frequency divider circuit. The mechanism effectively causes the output to toggle between one and 0 at a rate [*fr1] that of the input clock. therefore frequency division is achieved. The designed circuit and therefore the verification may be worn out TANNER EDA.

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