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Layout Impact of Resolution Enhancement in Design for Manufacturing (DFM) in submicron VLSI Design using Lithography Simulations

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Abstract: **As VLSI technology scales to 65nm and below, ancient communication between style and producing becomes a lot of and lighter. Gone square measure the times once designers merely pass the look GDSII file to the mill and expect excellent manufacturing and constant quantity yield. this is often for the most part thanks to the big challenges within the producing stage because the feature size continues to shrink. Thus, the concept of DFM (Design for Manufacturing) is obtaining highly regarded. even if there's no universally accepted definition of DFM, in my opinion, one in every of} the main elements of DFM is to bring producing info into the look stage in a means that's understood by designers. Consequently, designers will act on the knowledge to boost each producing and constant quantity yield. During this treatise, I'll gift many makes an attempt to cut back the gap between style and producing communities: Alt-PSM aware galvanic cell styles, printability improvement for careful routing and therefore the ASIC style flow with litho aware static temporal arrangement analysis. Experiment results show that greatly improve the manufacturability of the styles and that we can cut back style pessimism considerably for easier style closure.**

Keywords: **Layout, Cell, PSM, OAI, RSM, RET, SRAF, Optimization**

1. INTRODUCTION

For associate ASIC style, it accustomed be true that style and producing square measure comparatively independent of 1 another, with a collection of style rules the sole association between the 2. This configuration, however, is ever-changing as VLSI technology scales towards deep submicron technology nodes. Producing in sub-wavelength technology has become thus challenging that we want to deal with a number of the problems in style observe to boost producing yield. At a similar time, method variations within the advanced technologies cause either difficulty or superfluous pessimism for style closure. Clearly, a mechanism is required for modeling producing processes accurately and produces the modeling into style house. So styleer will effectively account for producing realities to reinforce manufacturing yield and at a similar time cut back design pessimism. During this treatise, i'll decide to gift a number of the new technologies to cut back the gap between style and manufacturing.

A. Alt-PSM Compliance and Composability for Standard Cell Layout

Current VLSI technology has the minimum semiconductor unit feature size of 90nm and 65nm, that is remarkably below the lithography wavelength of 192nm. The technology trend for future indicates that this gap can become even larger as shown in Figure one. Within the sub wavelength lithography, Resolution sweetening Techniques (RET) are deployed to com-bat robust diffractive effects that cause severe mate between mask shapes and written shapes. section Shifting Mask(PSM) is one among the common techniques in sop. PSM uses the damaging interference between 2 one hundred eighty degree out of section lights to print form edges.

There square measure 2 varieties of PSM presently in use, Attenuated PSM (Att-PSM) and Alternating PSM(Alt-PSM). In Att-PSM, mask substrates square measure accustomed enable a little quantity of the out of section light-weight to penetrate the unremarkably opaque mask regions. In Alt-PSM, lights with opposite phase's square measure shed on 2 sides of a skinny vital feature. Whereas Att-PSM poses less restriction in layout style than Alt-PSM will, Alt-PSM is less complicated to manage in lithography method and therefore the quality and therefore the strength of the written image is best. Alt-PSM is currently being employed in high performance VLSI styles in 90nm and 65nm technologies for its higher vital dimension (CD) management of semiconductor unit gate poly. For routing metals of the quality cell, Att-PSM might be used rather than Alt-PSM because the demand of CD management isn't as rigorous. Alt-PSM is also the sole possibility for section Shifting Mask of gate poly once VLSI technology additional scales down 45nm and 32nm. The Alt-PSM technique is illustrated in Figure.

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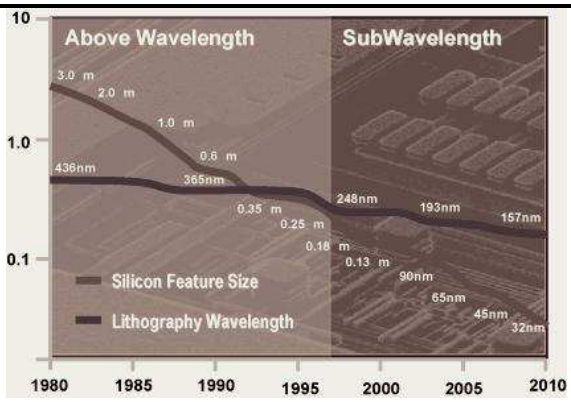


Fig. 1. Technology tread for transistor feature size

Even though the Alt-PSM technique is allotted within the stage of mask style and lithography, it has to be thought-about in circuit layout also. For instance, a T-shaped layout like in Figure could build section assignment unworkable. In[2], a section wherever a section conflict happens is split to change Alt-PSM as shown in Figure. Because the phases of lights square measure opposite on 2 sides of the cacophonous line (the dotted line in Figure), unwanted options is also left there and want to be cut by another exposure.

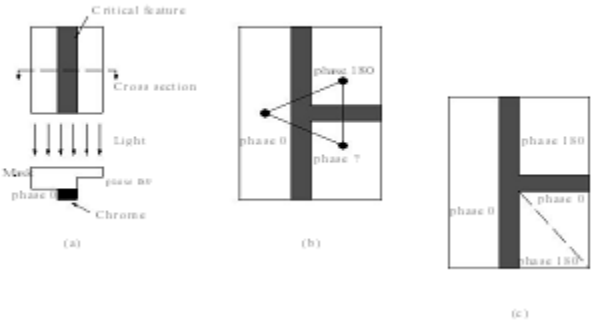
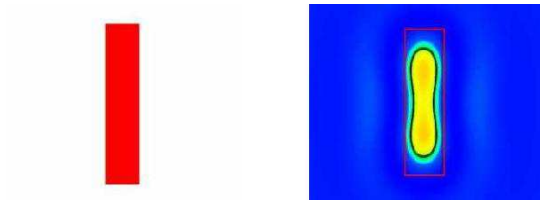


Fig. 2. (a) Alternating Phase Shifting Mask(Alt-PSM). (b) Phase conflict occurs for a T-shaped critical feature. (c) Phase conflict removal by splitting a phase region.

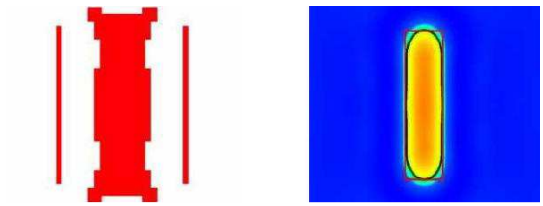
The second exposure can increase the already costly mask value and cause placement risk. Graph based mostly algorithms square measure projected to switch existing layout for Alt-PSM compliance. These algorithms can do world optimality, however demand massive computer hardware time if they're applied on a complete chip layout. what is more, it's terribly difficult to switch layout at prime level in galvanic cell based mostly styles, considering each mounted science styles and interactions between layout layers.

B. Wire Sizing and Spacing for Lithographic Printability and Timing Optimization

When lithography entered sub-wavelength regime, robust optical phenomenon impact could cause significant discrepancy between photo-mask patterns and written options. For instance, a parallelogram feature as in Figure on photo-mask could lead to written feature with distortion as in Figure on the Si. A circuit layout with poor printability implies that it's troublesome to form the written options on wafers follow designed shapes while not distortions. Currently, the printability of devices with sub-wavelength sizes is typically improved by using Resolution sweetening Techniques (RET) like Optical Proximity Correction (OPC), section Shift Mask (PSM), Off Axis Illumination (OAI), and Sub-Resolution Assist Feature (SRAF), thus on overcome optical phenomenon limit and method imperfections. for instance, mask layout for printing the parallelogram feature in Figure becomes Figure with OPC and SRAF. As a result, the written feature on Si (Figure) becomes nearer to the required parallelogram form.



(a) Traditional (b) Silicon image layout
Fig. 3. Layout without OPC and its silicon image



(a)Layout with OPC (b) Silicon image
Fig. 4. Layout with OPC and its silicon image

However, looking forward to sop alone is insufficient to harness the matter due to the subsequent reasons.

- The progressively massive gap between feature size and wavelength forces many aggressive RETs to be collectively applied and thereby compounds the already difficult mask style and will increase mask value drastically. Associate example in is shown in

Figure five to demonstrate this drawback. Compared to mask layout while not OPC like Figure 5(a), the mask layout with OPC like Figure 5(b) will increase mask knowledge volume, mask writing time and so mask value dramatically.

- The circuit complexness keeps growing and makes sop formidably difficult.

- RET deployments is also blockaded or maybe prohibited by associate RET-unfriendly lay-out. Therefore, the sub-wavelength printability drawback has got to be thought-about additionally in circuit layout style to confirm manufacturability.

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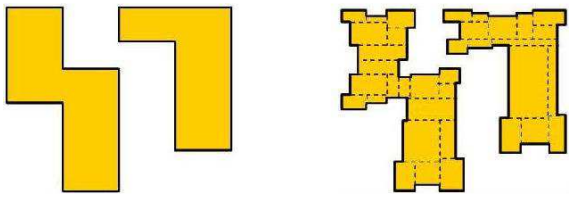

(a) Without OPC (b) With OPC
Fig. 5. OPC results in fractures in mask layout

In observe lithography friendly and/or sop compliant layout is usually obtained through either or model based methodology level approaches. In rule based mostly approaches, lithography friendliness and/or sop compliance square measure expressed as a collection of recommended/hard style rules that square measure applied in careful layout style like careful routing and layout compaction. This approach is quick and comparatively simple to use. However, lithography and sop procedures square measure thus difficult that it's terribly troublesome to convey their requests totally through easy rules. In model based mostly approaches, lithography and sop simulations square measure performed on a circuit layout and any determined issues square measure fed back to circuit designers for layout modification. The model based mostly solutions square measure usually a lot of reliable than the rule based mostly solutions, however the simulations square measure terribly time overwhelming and it always takes many iterations to achieve closure.

In order to beat the weakness of the methodology level approaches, lithography friendliness and/or sop compliance got to be thought-about directly in circuit layout algorithms.

C. ASIC Design Flow Considering Lithography Induced Effects

The International Technology Roadmap for Semiconductors (ITRS) comes that method variations gift a vital challenge for each producing yield and constant quantity yield of computer circuit merchandise. The method variations include systematic parts and random parts. The systematic variations represent each face Of Line (FEOL) and face Of Line (BEOL) parameter variations caused by inevitable style and method procedures, like CD (Critical Dimension) variations from totally different poly gate pitches and metal thickness variations occurred throughout Chemical Mechanical Planarization (CMP). Therefore, systematic variations behave deterministically normally.

In several existing style methodologies, folks sometimes treat systematic variations together with random variations while not differentiation. By handling each varieties of variations along in a very method corner based mostly methodology, folks will handily circumvent relatively complicated systematic variation models. However, such simplification sometimes causes superfluous pessimism in method corner estimations particularly once the systematic components account for an oversized portion of the variations. Indeed, it's reportable in that quite five hundredth of semiconductor unit gate length variations square measure thanks to systematic sources. As VLSI technology sharply scales to 65nm and on the far side, the influences from each systematic and random variations become bigger and bigger. The consequently increasing method corners force styleers to line aggressive temporal arrangement targets that intensify each design productivity crisis and power crisis . Therefore, important pessimism in method corner estimations isn't any longer tolerable and systematic variations got to thought-about otherwise from random variations.

Among systematic variations, gate length variation has maybe the biggest impact on circuit temporal arrangement and power performance since it directly affects each transistor shift speed and run power. Luckily, gate length variation for the most part depends on lithography method and might be captured through lithography/OPC (Optical Proximity Correction) simulations. A pioneer work tried to estimate gate length variations through computationally costly aerial image method simulations. Recently, a post OPC extraction methodology was projected for temporal arrangement analysis of vital ways in a very style. In, it's found that temporal arrangement vital ways square measure modified once post OPC extraction information is used. However, the temporal arrangement performance of a circuit isn't altered by this technique. Another work projected a temporal arrangement analysis methodology with awareness of lithography iatrogenic gate length variations per totally different poly pitches. For a regular cell, 3 poly spacing ranges square measure thought-about for its four boundaries and thereby eighty one variants square measure characterised for every cell. The temporal arrangement characteristic of a cell instance in a very layout is obtained by matching its encompassing layout pattern with one among the eighty one variants. Others projected a restricted style Rule (RDR) conception. This approach imposes a lot of demanding constriants on styles to reinforce producing yield. It essentially trades off style space and doable performance loss for fewer style variability.

In this chapter, we tend to gift a replacement galvanic cell characterization methodology considering lithography effects, then we tend to extend this discussion into BEOL to research the temporal arrangement impact of lithography effects on routing metals. supported these result, we tend to propose a replacement litho-aware temporal arrangement analysis flow that considers lithography iatrogenic effects on each gate length variations and interconnect wire dimension variations. During this methodology, the temporal arrangement and power performance of a cell relies on layout shapes obtained from lithography and OPC simulations and therefore the interconnect wire dimension variations is taken into account with a operation table.

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II. ALT-PSM COMPLIANCE AND COMPOSABILITY for normal CELL LAYOUT

Alternating section Shift Mask (Alt-PSM) has been known mutually of the necessary Res-olution sweetening Techniques (RET) solutions for producing of high performance styles due to its superior vital Dimension (CD) management of the written options. To facilitate the utilization of Alt-PSM in VLSI deep submicron producing, we tend to develop a replacement methodology for Alt-PSM aware library cell generation. We tend to project a two-way approach for library cell generation and a replacement library development flow that's terribly simple to incorporate into this style flow. The methodology we tend to projected guarantees that the highest level styles exploitation our Alt-PSM aware library don't have poly layer section errors, that is needed for producing with Alt-PSM.

In galvanic cell styles, one speeding methodology is to use the repetition usage of library cells. The Alt-PSM compliance for every library cell doesn't got to be obtained repeatedly, it will be achieved once in library cell styles. However, thanks to the proximity impact, putting Alt-PSM compliant cells adjacent to every alternative could cause new section conflict. For instance, in Figure vi, once the 2 Alt-PSM compliant cells square measure placed next to every alternative, section conflict can happen between the 2 regions indicated by the arrow.

We propose a 2 means approach for developing galvanic cell library with Alt-PSM compliance and composability. For smaller normal cells wherever placement of transistors has smallest impact on the electrical performance of the quality cell, we are going to construct cell layout to be Alt-PSM compliant and Alt-PSM composable; for larger standard cells with mounted semiconductor unit placement and routing for performance improvement,

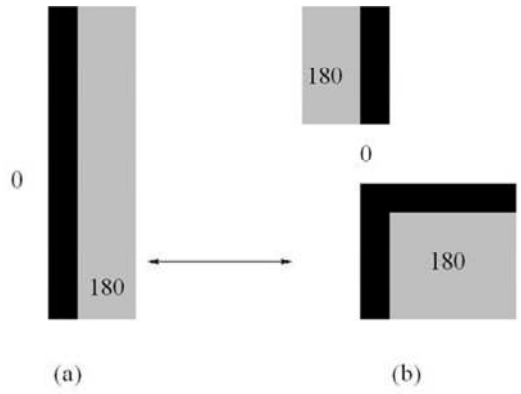

Fig. 6. Standard cell Alt-PSM composability.

We propose associate optimum and economical algorithmic program to switch the present layout to realize Alt-PSM compliance and composability.

For small galvanic cell construction, we tend to contemplate the semiconductor unit placement and intra-cell routing at a similar time in order that the layout of poly layer and metal layer will match with one another. As associate early classical work, Uehara and Cleemput developed a graph based mostly automatic cell layout system with a particular regular vogue. Recently, the minimum dimension version of the matter is tackled with Boolean satisfiability(SAT) methodology. We tend to additionally propose to realize Alt-PSM compliant and composable cell layout by exploitation Boolean satisfiability. We tend to remodel the constraints for the quality cell synthesis to a weekday formulation and so use encirclement weekday convergent thinker to look for answer. Our formulation handles multiple sized semiconductor units and considers transistor folding for giant transistors. For complicated normal cells, the location of the transistors has been optimized for performance, we tend to propose a network flow based mostly algorithmic program to switch the present layout for Alt-PSM composability with smallest cell space increase. Our experiments show that Alt-PSM necessities will be glad with efficiency at the science development level. Block level and prime level Alt-PSM compliance is secured by our methodology.

The paper is organized as follows: section two presents the weekday formulation for normal cell construction, section three provides the algorithmic program for normal cell layout modification. The experiment results square measure bestowed in section four. Section five is that the conclusions of this work.

Library Cell Construction: For simple normal cells with little range of transistors, we tend to use correct-by-construction approach for Alt-PSM compliant and composability. This section can gift the weekday formulation for normal cell construction.

III. WIRE SIZING AND SPACING FOR LITHOGRAPHIC PRINTABILITY AND TIMING OPTIMIZATION

The printability drawback thanks to robust optical phenomenon effects poses a significant threat to the progress of VLSI technology. A circuit layout with poor printability implies that it's difficult to form the written options on wafers follow designed shapes while not distortions. the event of Resolution sweetening Techniques (RET) will alleviate the printability drawback however cannot reverse the trend of degradation. Moreover, over-usage of sop could dramatically increase photo-mask value and increase the cycle time for volume production. Thus, there's a powerful demand to think about the sub-wavelength printability drawback in circuit layout styles. However, layout printability improvement shouldn't degrade circuit temporal arrangement performance. During this chapter, we tend to introduce a wire size and spacing methodology to improve wire printability with smallest adverse impact on interconnect temporal arrangement

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performance. a replacement printability model is projected to handle partly coherent illuminations. The complex printability and temporal arrangement improvement drawback is resolved in a very 2-phase approach. The problem of the printability improvement thanks to its multimodal nature is handled with a sensitivity based mostly heuristic. A coupling aware temporal arrangement driven continuous wire size algorithm is additionally provided. planographic printing simulation results show that our approach will improve the printability in term of EPE (Edge Placement Error) by two hundredth ¡ four-hundredth while not violating temporal arrangement, wire dimension and spacing constraints.

There square measure previous works to deal with DFM problems among style atmosphere. In, the Alternating PSM compliance is shapely as a graph drawback and layout modification algorithms square measure developed to realize Alternating PSM compliance with minimum value amendment. where the value will be outlined in term of space or temporal arrangement. Compared with Alternating PSM compliance, the opposite sop procedures square measure terribly troublesome to be abstracted into aphoristic models that may be simply embedded in automatic layout algorithms. Recently, the work of circumvents the troublesome sop abstraction issue by optimizing interference intensity in-stead, supported the observation that a reduced interference intensity can alleviate the employment of sop and therefore the interference intensity model is comparatively easier to be obtained. associate OPC friendly maze routing algorithmic program is projected in exploitation the interference intensity model. Associate sop aware routing algorithmic program supported quick litho simulation is projected in.

In layout printability optimizations, typical style objectives like temporal arrangement performance can not be unnoticed since temporal arrangement performance heavily depends on physical layout in todays interconnect dominated technology. During this chapter, we tend to specialize in the wire size drawback that plays a very important role on touching temporal arrangement performance and that we combine wire size and spacing to boost printability of the look. There square measure several previous works on wire size however largely for temporal arrangement improvement alone. The work of makes an attempt to reduce a weighted add of sink delays for a Steiner tree. A sensitivity based mostly wire size heuristic is reportable in. A dynamic programming based mostly coincident buffer insertion and wire size algorithmic program is projected in to realize timing-area exchange for a Steiner tree. A circuit-wise gate size and wire size methodology supported native refinement is developed in. In, the circuit-wise coincident gate size and wire size drawback is resolved optimally exploitation Lagrangian relaxation. A coincident wire size and spacing algorithmic program considering coupling capacitance is introduced in.

IV. ASIC DESIGN FLOW CONSIDERING LITHOGRAPHY INDUCED EFFECTS

In deep submicron VLSI styles, each temporal arrangement and power performance of integrated circuits square measure progressively full of method variations. In observe, folks typically treat systematic parts of the variations, that square measure usually traceable per method models, within the same means as random variations in method corner based mostly methodologies. In particular, lithography iatrogenic method variations square measure sometimes calculable by a universal worst case worth while not considering their layout atmosphere. Consequently, the method corner models supported such estimation square measure unnecessarily bearish. During this chapter, we tend to propose a replacement ASIC style methodology that captures lithography iatrogenic polysilicon gate length variations as well as each the layout dependent systematic parts and random components. Our methodology additionally shows that look-up table methodology is ample to handle BEOL (Back finish Of Line) lithography method variations in temporal arrangement analysis. Additionally, a replacement technique of dummy poly insertion is usually recommended to defend inter-cell optical interferences. This method in conjunction with normal cells characterized exploitation our methodology can let current style flows comprehend the variations nearly with none changes. a lot of significantly, by separating systematic lithography impact from random method variations, our methodology greatly reduces pessimism in temporal arrangement analysis, so permits each aggressive style implementation and easier temporal arrangement signoff. Experimental results on industrial styles indicate that our methodology will averagely cut back temporal arrangement variation window by 11 November, power variation window by fifty fifth compared to a worst case approach.

The main contributions during this work square measure as follows.

- A new technique of dummy poly insertion is usually recommended to handle the dependence of gate length variations on inter-cell spacing. In general, the gate length variations within the boundary regions of a cell depends on its spacing with fringe poly of neigh-boring cells. However, the neighboring cell info isn't obtainable before cell placement is completed. Our dummy poly insertion technique will usually avoid such dependence on unknown info. Therefore, we tend to don't got to characterize totally different variants of a cell as in [31]. Moreover, the pattern matching based mostly variant choice isn't necessary any longer in later style stages. In alternative words, the lithography aware cell characteristics will be used while not touching current standard cell based mostly style flows.

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- We utilize a poly segmentation technique to accurately assess every which way irregular poly shapes. The written poly shapes on wafer not solely have deviations on gate length, however even have deviations on different spots of a same poly. In alternative words, the deviations square measure by and enormous non-uniform. Our approach is in distinction to several previous works that treat the deviation of a poly uniformly.

- We verified that for lithography impact on wire dimension of interconnect, ancient operation table methodology remains valid.

- Accurate lithography simulations, as well as OPC, photoresist and print simulations, square measure temporal arrangement overwhelming normally. For sensible style use in temporal arrangement analysis, it's so terribly troublesome to run lithography simulations on the total chip level. However, the dimensions of a library cell are extremely little and therefore the characterization is typically performed just one occasion. Therefore, the costly lithography/OPC simulations square measure reasonable during this state of affairs. a lot of significantly, cell-based temporal arrangement annotation methodology is employed in typical temporal arrangement analysis for normal cell based mostly ASIC style. so as to not disturb this flow, it's so, terribly fascinating for a strategy to capture lithography impact in a very cell-based fashion. ancient ASIC

STA (Static temporal arrangement Analysis) flow utilizes method corner conditions for temporal arrangement signoff. This approach introduced high level of pessimism. for instance, in slow method corner, all semiconductor unit gates square measure assumed to possess the biggest gate lengths. In reality, which will ne'er hap-pen. due to the systematic nature for lithography effects, our methodology predicts this portion of the variations and take it into thought for STA to cut back pessimism considerably. we tend to applied our methodology to industrial library cell styles.

V. CONCLUSION

Design For Manufacturability (DFM) is seen as a vital channel of communication between style and producing for 65nm VLSI technology and on the far side. Our projected methodologies serve for the terribly purpose by translating producing info into style guidance that may be used by designers. we tend to addressed the problem of Alt-PSM section error within the galvanic cell development, we tend to improved the printability of the routing metals while not introducing temporal arrangement degradations, we tend to enabled the litho aware STA flow with litho aware galvanic cell characterization methodology. Hopefully, our efforts facilitate designers with success capture a number of the foremost necessary producing effects and so facilitate them to boost each producing and constant quantity yield of the look.

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