International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 1, Issue 9, September 2014)

Design and Simulation of Improved Memory Cell for Higher Read Stability

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***Abstract*—This paper presents a new CMOS 6T-SRAM Cell for various purpose including low power static RAM applications and stand alone static RAM applications. Using the same design rules and Technology the size of new 6T-SRAM Cell is comparable to the conventional SRAM cell. The conventional 6T SRAM cell shows lower stability at very small feature size with low power Vdd. The stability is low during the read operation, due to the voltage division between the access and driver transistors. Then we need to design a new SRAM cell, which also gives a proper degradation in SRAM cell data stability. In proposed solution we are proving that the new 6T SRAM cell what we are implementing in the proposed architecture which having higher stability and also we can see the power and area consumption comparable to the 180um Technology. During the write-read operation the new SRAM cell is operating by charging/discharging of a single ended bit-line (BL). All simulations process are done using by 130 nm Technology.**

***Index Terms*—Single ended bit-line, 6T SRAM Cell, read stable, SNM.**

I. INTRODUCTION

The semiconductor memory is generally classified according to the type of data storage and data access. Read/Write memory must permit the modification of data bits stored in the memory array, as well as their retrieval on demand. The read write memory is commonly called Random Access Memory (RAM), mostly due to its historical reasons. Unlike sequential access magnetic tapes, any cell can be accessed with nearly equal access time. Memories are said to be static if no periodic clock signals are required to retain stored data indefinitely. Memory cells in these circuits have a direct path to power supply or GND or both. Read-write memory cell arrays based on flip-flop circuits are commonly referred to as Static RAM or SRAM's.

The SRAM cell consists of a latch, therefore the cell data is kept as long as the power is turned on and refresh operation is not required. The static RAM is mainly used for cache memory in microprocessors, main frames and engineering workstations.

In the conventional 6T-SRAM cell shows lower stability at very small feature size with low power supply. During the read operation, the stability drastically decreases due to the voltage division between the driver transistor and access transistor. Since the Static Random Access memory (SRAM) cell operate on delicately balanced transistor. And the conventional 6T-SRAM cell, read stability is very low during read operation, it is very important to consider these issues during new memory cell design.

This project deals with design of low power Static Random Access memory (SRAM) cells with single bit-line, and focusing on stable operation and reduced read and write power .In this project, the focus is laid on the low power design of the SRAM, higher read stability than the standard one and reducing power consumption with addressing high-speed issues under low voltages. Further the power consumption is decreased by the switching operational voltage of the bit-line lies between 0.25VDD to 0.5VDD.

II. EXISTING SYSTEM

Static Random Access Memory (SRAM) cells have the advantages of faster access time and do not need the complication of periodically refreshing the memory cells compare to Dynamic Random Access Memory (DRAM). This is generally used when an application requires low idle power, or fast access time,or both. The SRAM is more expensive it uses 6T transistor as opposed to DRAM that only uses a transistor and a capacitor. So, SRAM is usually used in the part of design that the timing is critical such as processors cache.

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The existing six-transistor (6T) SRAM is built up of two cross-coupled inverters, two access transistors, two bit-lines and one word line ,which is tied between two access transistors shown in Fig 1.

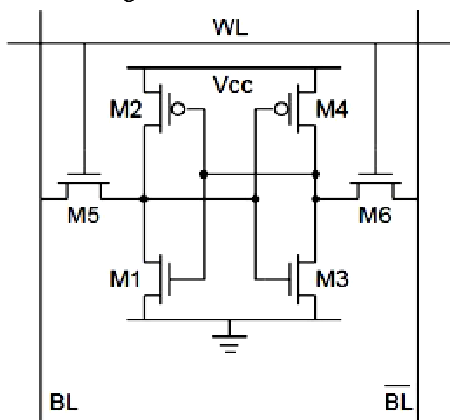

Figure 1. Standard 6T-SRAM Cell

In 6T-SRAM Cell, the two cross coupled inverters make up the storage element and the transistors M5 and M6 act as a access transistor. These transistor are used to access the stored data in the cell and turned ON/OFF by the control line called word-line (WL). When wordline is charged the cell is connected to bitline and complement of bit line (BLbar) allowing both write and read operations. The read and write operations is carried out by the help of access transistor. The SRAM cell is symmetrical and has a relatively large area. No special process steps are needed and it is fully compatible with standard CMOS processes.

This 6T-SRAM cell shows low stability at very small feature size with low power supply. The stability is drastically reduced during the read operation due to the voltage division between the Access transistor and Driver transistor. During the read operation, the Cell stability in the storage invertors are usually made strong and pass-gates are weak. Similarly in the write operation, the storage invertors are weak and strong pass-gates.

A. SRAM Cell operations

Read Operation: The standard 6T-SRAM cell has a differential read operation. This means that both the stored value and its inverse are used in evaluation to determine the stored value. Before start of a read operation, the Word line is getting low (grounded) and the two bit-lines connected to the cell through transistors M5 and M6 (see Figure1) are precharged high (to VCC). Since the gates of M5 and M6 are held low, these access transistors are off and the cross-coupled latch is isolated from the bitlines.

If a 0 value is stored on the left storage node, the gates of the latch to the right are low. That means, Transistor M3 (see Figure 1) is initially turned OFF. In the same way, M2 will also be OFF initially since its gate is held high. This results in a simplified model, shown in Figure 2, for reading a stored 0.

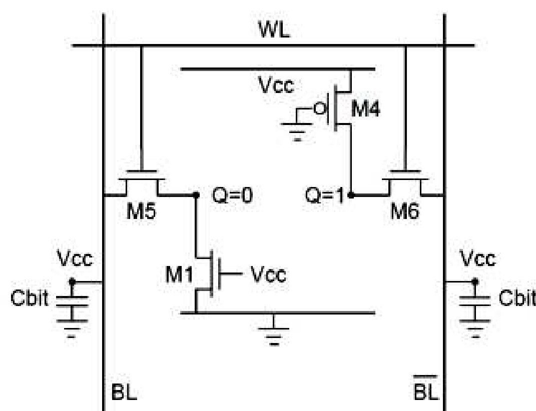

Figure 2. Read operation(reading ‘0’) of 6T-SRAM cell

The Cbit represent the capacitances of the bitlines (fig 2), which are several magnitudes larger than the capacitances of the cell. The cell capacitance has been represented only through the value held by each inverter (Q=0 and Q=1 respectively). The next phase of the read operation scheme is to pull the Wordline (WL) high and at the same time release the bitlines. This turns on the access transistors (M5 and M6) and connects the storage nodes to the bit lines. It is evident that the right storage node (the inverse node) has the same potential as BL and therefore no charge transfer will be take place on this side. This process develops a voltage difference between the two nodes which is sensed by sense amplifier to detect it as ‘1’. Similarly a ‘0’ in the cell it also detected by the sense amplifier.

Write Operation: Consider to write 0 to the cell, BL line held low and BLbar line is raised to Vcc by the write circuit which is shown in Figure 3. Thus the node Qbar (Q=1) is pulled up towards the Vcc/2 while node Q (Q=0) is pulled down to Vcc/2. When the voltage crosses this level on two nodes, feedback action starts.parasitic capacitances developed by M1,M5 and M4,M6 are charged and discharged respectively.

If the node is raised, transistor M1 will sink current to ground and the node is prevented from reaching even close to the switching point. So, a 0 value is written to the inverse node instead of writing a 1 value . Looking at the right side of the cell we have the constellation M4-M6. In this case BL is held at ground. When the Wordline (WL) is raised M6 is turned on and current is drawn from the inverse storage node to BL. However, At the same time M4 is turned on and as soon as the potential at the inverse storage node starts to decrease current will flow from VCC to the node. In this case M6 has to be stronger than M4 for the inverse node to change its state. The transistor M4 is a PMOS Transistor and inherently weaker than the NMOS transistor M6 (the mobility is lower in PMOS than in NMOS).

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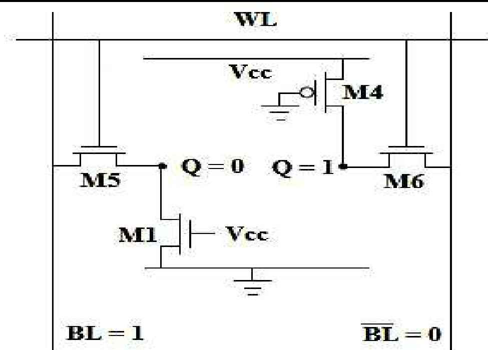

Figure 3. Write operation (writing ‘0’ or ‘1’) of 6T-SRAM cell

B. Limitation of standard SRAM cell

A standard 6T-SRAM cell has poor read stability as technology scale down to nano-regime. By increasing the bitcell ratio, the power consumption and write increases which incur loss of power and performance, and also increase in area overhead (as shown in Table 1). The 6T-SRAM bitcell fails to operate in sub-thershold voltage (Vth).

Table I. Variation in different parameters of standard 6T with bitcell ratio

Bitcell ration	1	1.5	2	2.5	3
SNM (Mv)	27.4	60.7	79.7	91.9	102.3
Write Time (ps)	35.38	42.25	47.48	52.17	57.15

From the above table1, we can conclude that by increasing the cell ratio, we can improve read SNM and at the same time there is increase in write time.

III. PROPOSED SYSTEM

The proposed new six-transistor (6T) SRAM cell is made up of single bit-line (BL), one wordline (WL), two pull-up (PMOS) and pull-down (NMOS) transistors. The two NMOS transistor (M3 & M5) are known as Pass-transistor. These Pass-Transistors are used to transfer the data from bit-line (BL) to Cell and from Cell to bit-line (BL). The schematic of new 6 transistor (single ended) SRAM cell is shown in Figure 4.

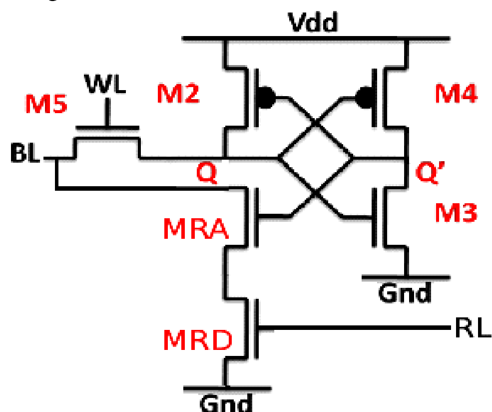

Figure 4. Proposed 6 transistor (single ended) SRAM Cell

The Proposed new single ended 6T-SRAM cell is created by adding two more transistor i.e, MRA (Read Access Transistor) and MRD (Read Driver Transistor). These transistors are work independently during read operation and won’t effect the cell Static Noise Margin (SNM) in anyway.

The Proposed technique is existing from standard 6T-SRAM cell shown in Figure 1.In that 6T-SRAM cell the transistor M6 is taken away, which still works like a 6T-SRAM . The advantages is decrease in cell area and power consumptiom. The cell area is decreased by one transistor and also decreased by one bit-line (BL). Hence the power consumption from charging the bit-line decreases by approximately a factor of 2 because instead of two bit-lines (BL) only one bit-line is charged during the read operation. During the write operation the bit-line is charged about half of the time (assume equal probability of writing 0 and 1) instead of every time when a write operation is required.

Again the transistor M1 is being removed from the schematic like Figure 1 if obtained, which also works same as the functionality of a SRAM and the main advantages of that design is further reduction of power consumption. And the other advantages is include the significant larger write margin and smaller delay for writing 1,and slightly smaller cell area.

Finally in the proposed single bitline 6T-RAM cell, adding a two transistor (MRA,MRD), which should be serially connected in the place of Transistor M1 . In that the transistor MRA is connected to bit-line (BL) and MRD is directly connected to ground. The read line (RL) is placed in the gate of Read Driver Transistor (MRD). Read line RL is act like a controller.

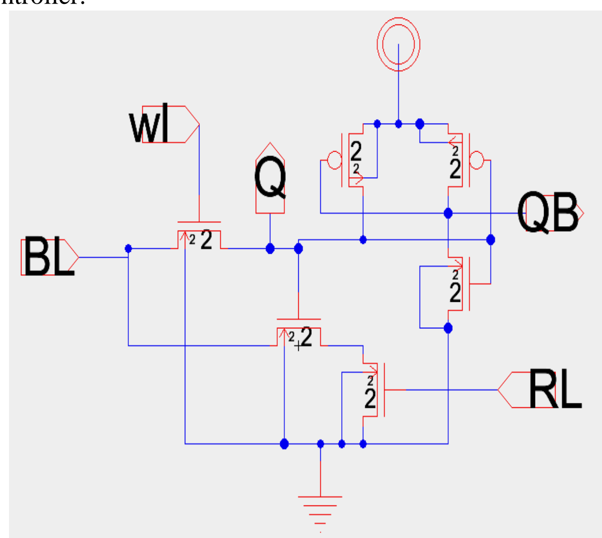

Figure 5. Schematic of Proposed single bit-line 6T SRAM Cell in Electric VLSI Design System

The proposed Cell uses a single bit-line (BL) and operates the charging/discharging of single BL during read-write operation. Resulting in reduction of dynamic power

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consumption and has higher read stability than the standard SRAM cell. Also increases the Static Noise Margin (SNM).

Further the power consumption is decreased, if the switching operational voltage of the bit-line (BL) lies between 0.25 Vdd to 0.5 Vdd. The proposed new 6T-SRAM cell for different purposes including low power embedded SRAM application and stand-alone SRAM application.

A. Memory Cell Operatons

- **HOLD:** If the cell content is a 1 (Q=VDD, Q'=0), both memory nodes will lock each other at their respective voltages. However, if the cell content is a 0 (Q=0, Q'= VDD), Q is floating. Referring to Figure 4, the leakage current through M5 must be greater than that of M2 to ensure Q stays at 0. Fortunately, since NMOS (M5) is a stronger current driver than PMOS (M2), this condition is satisfied.

- **WRITE:** The word-line WL is charged to VDD as in 6T Standard SRAM. Since NMOS is a stronger driver than PMOS, no problem is incurred while writing a 0 into the cell. The absence of the pull down NMOS for memory node Q allows writing a 1 into the cell easily. Writing a 1 is done by pre-charging bit-line BL to VDD. While writing 0, the bit-line BL is discharged and then word-line WL is charged to VDD as in 6T Standard SRAM.

- **READ:** Considering the case of reading Q=0; before reading a value from the storage nodes, the bit line BL is pre-charged to VDD. The read word line RL is then asserted to VDD. The storage node Q' that stores a 1 is statically connected to the gate of MRA (Read Access Transistor) and will drain the charges on the bit line through MRD to GND as the RL is 1, which means that the bit line has just read a 0. On the contrary, when Q=1, Q' will be 0 and MRA will be in cutoff and the bit line BL would not be able to discharge through MRD to Gnd, and it would read a 1.

IV. SIMULATION RESULTS

A. Dynamic Power Consumption

There are two phases for power consumed in an SRAM operation, the operational phase and the setup phase.

During the operational phase power consumed is dominated by leakage power and active power. The power consumed when the charges 'leak' through a transistor is called Leakage power ,ans that is OFF. The power consumed when both (NMOS, PMOS) pull-down and pull-up networks are active is called Active power, and creating a direct current path from VDD to GND.

During the setup phase power consumed is dominated by charging/discharging various buses like as bit lines (BL) and word lines (WL). Using the formula $E_{Line} = 0.5 * C_{Line} * V_{Line}^2$,in which V_{Line} is the change in line voltage and C_{Line} is the line capacitance. From this information the average power of an SRAM operation is obtained by dividing the clock period.

Therefore, consumed power $P_{line} = C_{Line} * V_{Line}^2 * F$

If switching activity and clock frequency is reduced then the dynamic power dissipation can be lowered but it affects the performance. The cell data stability is degraded by reduction of supply voltage. So, the dynamic power dissipation can be decreased by reducing bitline capacitance of SRAM cell without affect the performance.

Table II. Calculated Switching Power

charging and discharging of single Bit-line considered

	6T Standard SRAM Cell	Proposed 6T SRAM Cell
WRITE 0	162uW	0uW
WRITE 1	162uW	81uW
READ 0	243uW	162uW
READ 1	243uW	81uW

In the proposed new 6T-SRAM Cell, only a single bit-line is charged when the value is 1 and does not get charged at all assuming that the data was already present before the precharge circuit has been activated. After the write 1 operation, the bit-line is assumed to get discharged. During a read 0 cycle, the bit-line capacitance is pre-charged and discharged through the cell, where as in a read 1 cycle, the bit-line is pre-charged and assumed to be discharged after the read process is over.

Table III. Calculated Average Power

SRAM Cell	Average Power
4T-SRAM	1.3525 uW
5T-SRAM	3.2355 uW
6T-SRAM	4.5875 uW
Proposed 6T-SRAM	266.45 nW

B. Delay Calculation

The main operations of the SRAM cell are the write, read and hold. The static noise margin is certainly more important at hold and read operations [6], specifically in read operation

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when the wordline is 1 and the bitlines are precharged to 1. The internal node of SRAM which stores 0 will be pulled up through the access transistor across the access transistor and the driver transistor. This increase in voltage severely degrades the SNM during read operations. During read/hold operation, the requirement is that the SRAM cell must be as robust as possible so that a sudden disturbance will not change the content in the memory nodes.

The delays of SRAM are usually defined by the time it takes to read or write a value from an SRAM cell. When a transistor is switching the delay is measured as the time difference between 10% and 90% of the voltage swing.

Assume, in the simulation that the bit-lines have 1pF capacitance which is much higher a value than node capacitance at VNode1. Therefore, it takes much less effort to switch memory nodes than to switch bit line. That's why in general, delays for write operation are smaller than that of read operation in SRAMs, because writing into a cell is the same as switching the memory node, and reading from a cell is the same as switching the bit line.

The smallest write 1 delays are shows in the proposed 6T-SRAM design, because there is no pull down NMOS that keeps the memory node from being pulled up to Vdd. And also the wrost write 0 delays because there is no pull down NMOS that helps to being the memory node to 0.

Table IV. Delay Analysis Results

	6T Standard SRAM Cell	Proposed 6T SRAM Cell
WRITE 0	5.1 nS	6 nS
WRITE 1	5.5 nS	0 nS
READ 0	7.5 nS	8.5nS @ 600nM 6.5nS @ 800nM {MRD/MRA}

C. Static Noise Margin

SNM is the measure of stability of the SRAM cell to hold its data against noise. SNM of SRAM is defined as minimum amount of noise voltage present on the storing nodes of SRAM required to flip the state of cell. Increases the cell stability has been done in proposed 6T-SRAM cell circuit for future technology nodes [14].

In the standard 6T SRAM cell the read static noise margin is much affected with decrease in supply voltage and transistor mismatch [12], [16]. This mismatch happens due to variations in physical quantities the devices designed to be identical. Commonly known physical quantities are threshold voltages, body factor and current factor. Though SNM decreases at low VDD the overall delay of the SRAM increases and also data destruction takes place with low VDD read operation in SRAM cells [12]. In the proposed SRAM cell, reading from the cell has no effect on the static noise margin because the data retention and the data output blocks are isolated.

During read and hold operation, the requirement is that the SRAM cell must be as robust as possible so that a sudden disturbance will not change the content in the memory nodes. For example, read noise margin of 200mV means that during read operation, if one of the memory nodes (Q or Q') changes by less than 200mV, then we can be sure that after the read operation, the content of Q and Q' will remain the same, and any disturbance to the voltage in the cell will be eliminated. Therefore, a larger read/hold noise margin is preferred. During write operation, the situation is reversed; the requirement is to switch the content of Q and Q' easily. Therefore, the write noise margin (more commonly referred to as the "write margin") is defined as the range of voltage disturbances that will flip the content of the memory nodes. For example, if write margin is 500mV, then a range of at least 500mV disturbance in the memory nodes will cause their content to flip, thus achieving write operation

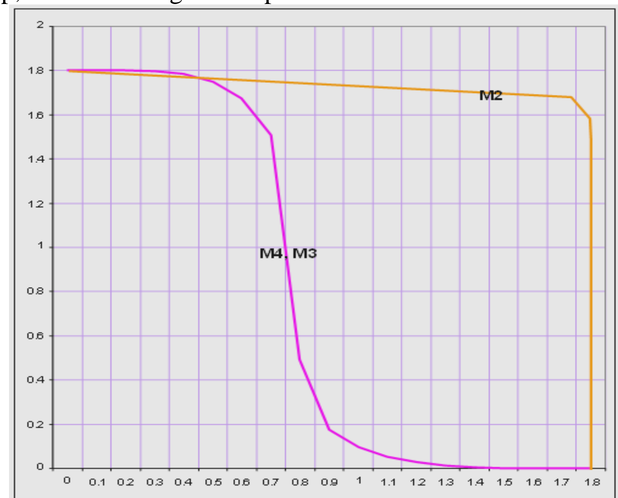

Figure 6. Hold state SNM curve for the proposed 6T-SRAM Cell

In the proposed single ended 6T SRAM cell, reading from the cell has no effect on the Static Noise Margin (SNM) because the data retention and the data output blocks are isolated.

C. Simulation waveforms for Proposed 6T-SRAM Cell

The proposed single ended 6T-SRAM cell consumes less dynamic power which is shown in Figure 7. The average power is decreases comparable to the standard SRAM cell. Hence , the power is reduced from micro watts (uW) to nano watts (nW). The proposed design increases the higher read stability by using single bit-line and also increase the speed of the system.

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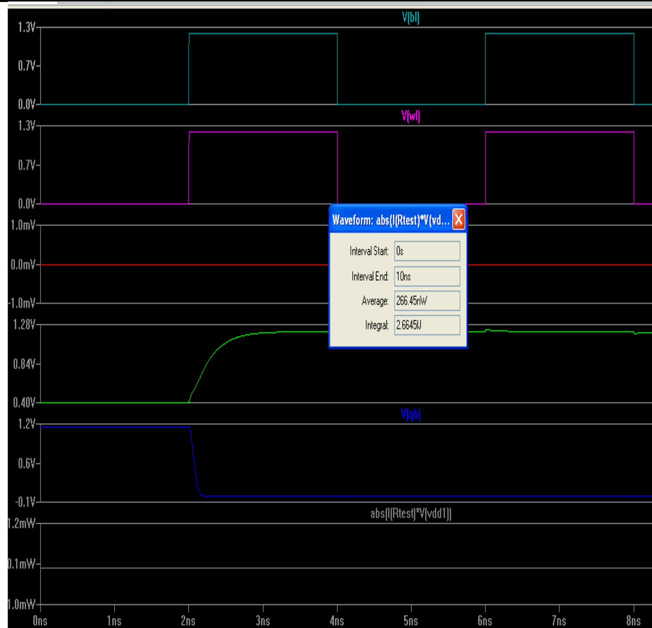
Figure 7. Proposed Result for Single ended 6T-SRAM Cell

V. CONCLUSION

Rapid development of increasing the technology scaling puts a limit on how much supply voltage can be scaled. Therefore, reducing the power consumption with new design requirements in recent integrated circuits (IC). In the case of SRAM, the proposed design approach is to utilize a single bit-line without affect the read stability, which leads to the development of a Single Ended 6T SRAM. The new 6T-SRAM design operating system, performs a accurate power reduction by decreasing the number of switching on bit- lines. To extending this design allows us to propose a single bit-line design that achieves a relatively smaller area while retaining all of the power saving advantages. The proposed design technique is maximizing the access speed of new SRAM Cell with minimal power consumption to optimize the overall system performance.

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