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Design of a Low Power and High Performance Digital Multiplier Using a 6T Adder

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Abstract: **Low power VLSI circuits have become important criteria for designing the energy efficient electronic designs for high performance and portable devices .The multipliers are the main key structure for designing an energy efficient processor where a multiplier design decides the digital signal processors efficiency. Multiplier is the most commonly used circuit in the digital devices. Multiplication is one of the basic functions used in digital signal processing. Full Adder is the main block of power dissipation in multiplier. So reducing the power dissipation of full adder ultimately reduces the power dissipation of multiplier. In this paper proposes the novel design of a 2T XOR gate. An 6-T full adder has been designed using the proposed 2-T XOR gate and its performance has been obtained. In this paper a XOR gate using two transistors has been presented. A single bit full adder using six transistors has been designed using XOR cell, which shows power dissipation of 620.5µ W. A 4x4 Wallace tree multiplier has been implemented by using the proposed 8T adder. Simulations have been carried out by using cadence tool based on gpdk180nm CMOS technology**

***Keywords*- CMOS, exclusive-OR (XOR), exclusive-NOR (XNOR), full adder, low power, multiplier.**

I. INTRODUCTION

The prolific growth in semiconductor device industry has lead to the development of high performance portable systems with enhanced reliability in data transmission. In order to maintain portability of high-performance fidelity applications, emphasis will be on incorporation of low-power modules in future system design. The design of such modules will have to partially rely on reduced power consumption and/or dissipation in fundamental arithmetic computation units such as adders and multipliers. This underscores a need to design low power multipliers towards the development of power-efficient high-performance systems.

The increasing demand for the high fidelity portable devices has laid emphasis on the development of low power and high performance systems. In the next generation processors, the low power design has to be incorporated into fundamental computation units, such as multipliers. The characterization and optimization of such low power multipliers will aid in comparison and choice of multiplier modules in system design. With exponential growth of portable electronic devices like laptops, multimedia and cellular device, research efforts in the field of low power VLSI (very large-scale integration) systems have increased many folds. With the rise in chip density, power consumption of VLSI systems is also increasing and this further, adds to reliability and packaging problems. Packaging and cooling cost of VLSI systems also goes up with high power dissipation. Now a day's low power consumption along with minimum delay and area requirements is one of important design consideration for IC designers.

spurious transitions[7– 8]others have focused on developing novel multiplier architectures and sign-extension techniques to reduce power dissipation and improve performance[3][9].The selection of the most efficient architecture to implement multiplication has continually challenged DSP system designers. The options currently available offer a wide range of tradeoffs in terms of speed, complexity and power consumption. Input sequences to the multiplier can be fed in parallel, serial or a hybrid (parallel-serial) approach. To achieve higher processing speeds, Parallel multipliers are usually adopted at the expense of high area complexity. Multiple parallel multiplication algorithms (architectures) [2][6] have been proposed to reduce the chip area and increase the speed of the multipliers. Various techniques have been developed to reduce the power dissipation of parallel multipliers. While several of these techniques reduce power dissipation by eliminating

Yet another approach is to develop low-power 3–2 counters and 4–2 compressors, which are key components in parallel multipliers [10]. Although each of these techniques helps reduce power dissipation, further reductions will be needed for future digital signal processing systems. This research uses an approach to significantly reduce the power consumption and the chip area of the parallel multipliers, without sacrificing performance. The approach is based on using low power, minimal transistor count adders that are the determining blocks (second stage of algorithm) in the performance of the multiplier. The operation of a parallel multiplier can be divided into two parts:(a) formation of the partial products, and (b) summation of these products to form the final product of the multiplication. Binary addition is basic and most frequently used arithmetic operation in microprocessors, digital signal processors (DSP) and application-specific integrated circuits (ASIC) etc. Therefore, binary adders are

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crucial building blocks in VLSI circuits and efficient implementation of these adders affects the performance of entire system[5].

II.BACKGROUND

2.1. MULTIPLIER ARCHITECTURE

The multipliers play a major role in arithmetic operations in digital signal processing applications. The present development in processor designs aim at low power multiplier architecture usage in their processor circuits. So, the need for low power multipliers has increased. Hence the designers concentrate more on low power efficient circuit designs. Generally the computational performance of dsp processors is affected by its multipliers performance. Hence we put over a solid care to overcome those drawbacks using our design. Processors efficiency is usually determined from its multiplier speed and supply voltage. Booth algorithm and Wallace tree counters or compressors are the basic algorithms used to increase the speed of the parallel multipliers[1]. Thus to speed up the processor mostly a parallel multiplier can be used comparative to serial multipliers for better performance. But the demerit in the booth algorithms style is its high energy dissipation. Hence we go for a Wallace tree multiplier which is designed by using 6T adder.

If speed is not an concern in multiplier designs then partial products can be summed serially to reduce the risk of design complexity but speed and low power has became an important criteria in designing today's energy efficient processors. Hence the Wallace tree multiplier structure is used to add up all the partial products of the bits by parallel multiplication [4]. Thus, it is said to work in parallelism. In this method the bits in each column are compressed into two bits. Here an adder itself works as an compressor where it compresses three input bits to two output bits where the output one bit is the carry bit of weight n+1 and the sum bitof weight n. Hence it is said to be 3:2 compressor or counter and its multiplication style is shown in fig1. In this paper the multiplier is designed using 6Tadder.

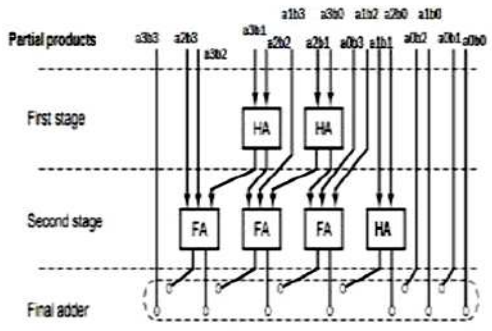

Figure1: Wallace tree multiplier design flow

Multipliers can be implemented using different algorithms. Depending on the algorithm used, the performance characteristics of the multipliers vary. In the implementation of digital multipliers binary adders are an essential component. With the emergence of power as a design consideration, speed is not the only criterion by which various implementations are judged. Designing multipliers with low power, energy efficient adders reduce the power consumption and efficiency of multipliers.

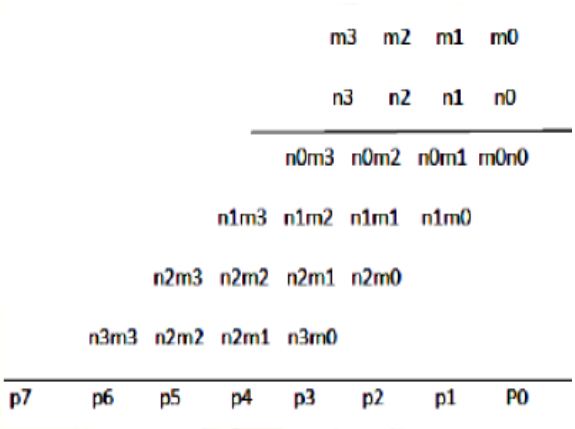

Figure2: Multiplication of 4*4 bit numbers

Wallace trees were first introduced in 1964 in order to design the multipliers whose completion time grows as the logarithm of the number of bits to be multiplied increases. Wallace tree multiplier is based on tree structure. In Fig1 a 4 bit Wallace tree multiplier is shown. Wallace method uses three-steps to process the multiplication operation

1) Formation of bit products

2) The bit product matrix is reduced to a 2-row matrix by using a carry-save adder (Wallace tree).

3) The remaining two rows are summed using a fast carry-propagate adder to produce the product.

The advantage of Wallace tree is speed because the addition of partial products is O (log N) where N is the number of summands

III. CHARACTERISTICS OF MULTIPLIERS

There are three main components of power consumption in digital CMOS VLSI circuits.

1) **Switching Power:** consumed in charging and discharging of the circuit capacitances during transistor switching.
2) **Short-Circuit Power:** consumed due to short-circuit current flowing from power supply to ground during transistor switching. This power more dominates in Deep Sub Micron (DSM) technology.
3) **Static Power:** consumed due to static and leakage currents flowing while the circuit is in a stable state. The first two components are referred to as dynamic power, since power is consumed dynamically while the circuit's changing states. Dynamic power accounts forthe majority of the total power consumption in digital CMOS VLSI circuits at micron technology [11][12].

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$$P_{avg} = P_{dynamic} + P_{static} = (P_{Switching} + P_{Short\text{-}Circuit}) + P_{Leakage} = (\alpha_{0\to1} \times C_L \times V_{dd}^2 \times f_{clk}) + (I_{sc} \times V_{dd}) + (I_{leakage} \times V_{dd}) \quad (1)$$

The first term and second term in (1) collectively represents the dynamic power. Under the circumstance of 180nm the static power loss is far less than its counterpart—dynamic power dissipation. Therefore, in most cases, the total power loss is approximate to dynamic power consumption, which is also considered to be related to the internal node capacitance and the probability of switching.

IV. SYSTEM DESCRIPTION

DESIGN OF THE SIX-TRANSISTOR FULL ADDER

The new design of full adders[7][11] which forms the basic building blocks of all digital VLSI circuits has been undergoing a considerable improvement, being motivated by three basic design goals, viz. minimizing the transistor count, minimizing the power consumption and increasing the speed.

x + y + Cin =2Cout + Sum
Cout =(y(x ⊕ y)) + (Cin(x ⊕ y))
Sum = x ⊕ y ⊕Cin

The static CMOS Full adder is implemented by using 26 transistors. we can also minimize the number of transistors by using the CMOS Transmission gate and CMOS inverter. With this logic we reduce the number of transistors to 20.By using Pass transistor logic we can minimize the static power dissipation and number of transistors. Full adder is design with 14 transistors[9] by using Pass transistor logic which leads the moderate power dissipation. The full adder design also implemented by using 10 transistors[6]

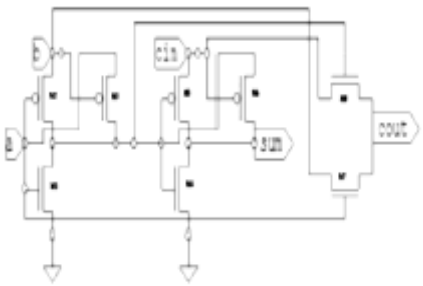

Fig.2: Previous designs of 8T Full adder.

Mainly the XOR[8] and XNOR circuits are used in designing of full adder. In previous design the Full adder is designed by using eight transistors which can dissipates more power compare to this work.In this paper the design of full adder using two transistors xor gates can be implemented. The Six transistor Full adder is shown in Figure.3

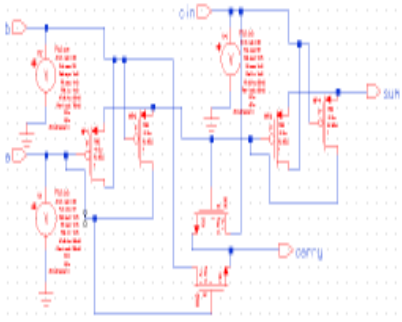

Fig.3: Proposed Design of 6T – Full adder

Structure	No. of transistors	Power(µw)
Full Adder	8	0.367
Full Adder	6	0.235

Table 1: Power consumption of 8T and 6T FA

V. SIMULATION RESULTS

a) Input and Output Waveforms of Full Adder

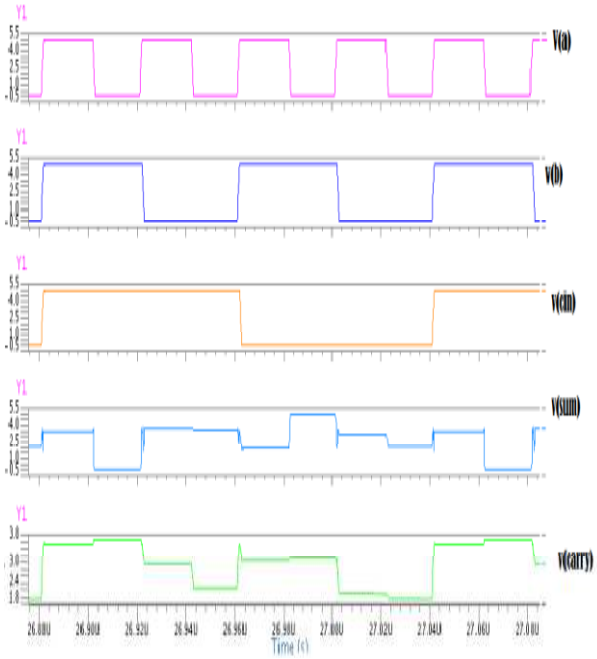

Fig.4.Wave form of 6T-Full adder

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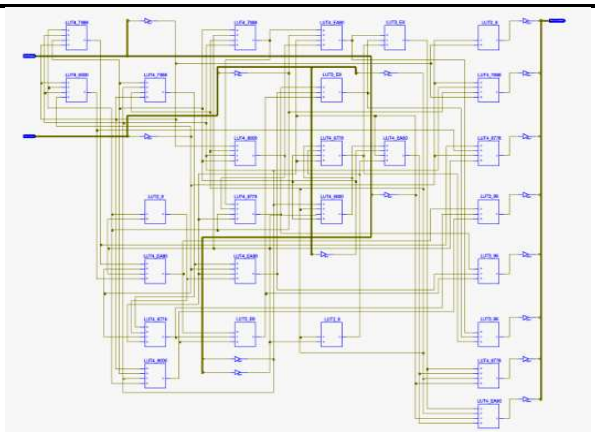

Fig5.Wallace tree multiplier

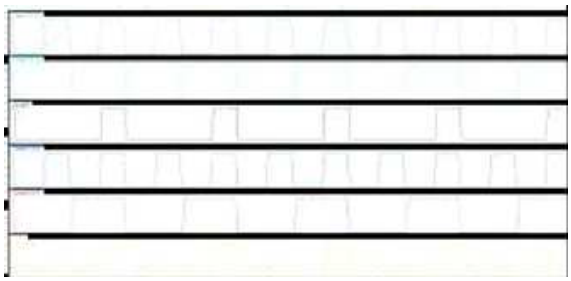

*Fig*6: Input and output waveform of Wallace tree multiplier

c) Expected Power Dissipation and Delay for Full Adder and Wallace Tree Multiplier

Table2: Power and Delay of Full Adder and Wallace Tree Multiplier

Structure	Power Dissipation	Delay
Full Adder	< 620.2(µw)	<22.0e-9
Wallace Tree Multiplier	< 18.3(mw)	< 31.3e-9

CONCLUSION

To design energy efficient Wallace tree multipliers, use of full adders not only reduces the critical path but also usages of energy efficient adder designs make them the best for higher order circuits and processors. Hence better performances of the multipliers are tested with efficient adders. A single bit full adder using six transistors has been designed using proposed XOR cell, which shows power dissipation less than 620.5µW. A 4x4 Wallace tree multiplier has been implemented by using the proposed 6T adder, which shows a power dissipation less than18.23mw.Power consumption of proposed XOR gate and full adder circuit's shows better performance in terms of power consumption and transistor count.

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