

# Design and Characterization of High Speed Carry Select Adder

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**Abstract**— Adders are the basic building blocks in digital integrated circuit based designs. Ripple Carry Adders (RCA) are usually preferred for addition of two multi-bit numbers as these RCAs offer fast design time among all types of adders. However, RCAs are slowest adders as every full adder must wait till the carry is generated from previous full adder. On the other hand, Carry Look Ahead (CLA) adders are faster adders, but they required more area. The Carry Select Adder(CSLA) is a compromise on between the RCA and CLA in term of area and delay. This paper presents High Speed Carry Select Adder by replacing Ripple Carry Adder with Kogge-Stone(KSA) Parallel Prefix Adder. Based on this modification 8, 16, 32 and 64-bit High-Speed Proposed Carry Select Adder (PCSLA) architectures have been developed and compared with the Regular and Modified CSLA architectures in Uniform and Variable Block Size. This work estimates the performance of the proposed designs in terms of Maximum combinational delay, Logic delay and Routing delay which are designed and implemented in Xilinx ISE tool.

**Index Terms**— Binary to Excess-1 Converter, Carry Select Adder, Delay, Kogge- Stone Parallel-Prefix Adder, Multiplexer, RCA.

## I. INTRODUCTION

Binary Addition is the most fundamental arithmetic operation. It has been ranked the most extensively used operation among a set of real-time digital signal processing benchmarks from application-specific DSP to general-purpose processors. In particular, carry-propagation adder (CPA) is frequently part of the critical delay path limiting the overall system performance due to the inevitable carry propagation chain. The speed of addition is limited by the time required to propagate a carry through the adder[1]. The CSLA is used in many computational systems to moderate the problem of carry propagation delay which compromises between RCA and CSLA. The CSLA requires dual RCAs in which RCA with "Cin=1" replaced by BEC improves delay and area. The CSLA using variable block sizing, the delay can be further reduced[2]. To increase the speed of CSLA, Parallel Prefix Adder is used instead of RCA. The Kogge-Stone Adder is chosen due to low critical path and maximum fan-out. The High Speed Regular and Modified CSLA is designed using Kogge-Stone Adder by replacing RCA with "Cin=0". The details of Ripple Carry Adder, Multiplexer, Binary to Excess -1 Converter and Carry Select Adder are

discussed in Section II, the complete functioning of Kogge-Stone Adder is discussed in section III, The implementation of High Speed Proposed CSLA architectures in Uniform and Variable block size is described in section IV. The performance and simulation results are presented and discussed in section V.

## II. CARRY SELECT ADDER

In Electronics, Carry-Select adder is a particular way to implement an adder. It generally composes of two Ripple Carry Adders with carry 0 and 1 and a multiplexer.

### Ripple Carry Adder

Ripple Carry Adder consists of cascaded "N" single bit full adders. Output carry of previous adder becomes the input carry of next full adder. Therefore, the carry of this adder traverses longest path called worst case delay path through N stages. Fig. 1 shows the block diagram of Ripple Carry Adder. Now as the value of N increases, delay of adder will also increase in a linear way. Therefore, RCA has the lowest speed amongst all the adders because of large propagation delay but it occupies the least area.

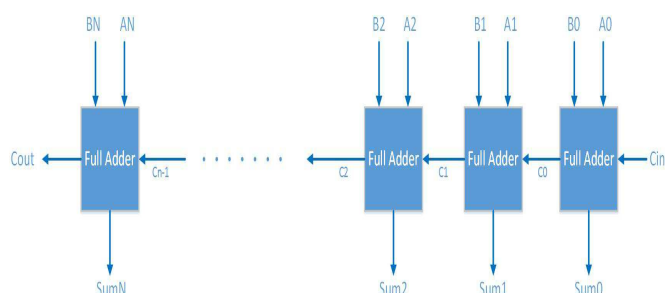


Fig. 1. N-bit Ripple Carry Adder.

### Multiplexer

In digital electronics, a multiplexer (or mux) is a logic element that selects one of several digital signals and forwards the selected input into a single line A multiplexer of '2<sup>n</sup>' inputs has 'n' select lines, which selects which are used to which input line to send to output. It is also widely known as many to

one circuit, data selector and universal parallel to serial converter. The 8:4 Multiplexer is shown in Fig. 2.

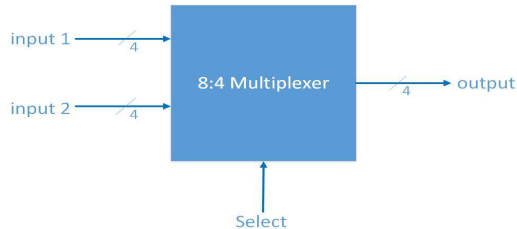


Fig. 2. 8:4 Multiplexer.

## Binary to Excess-1 Converter

The basic work is to use Binary to Excess-1 Converter (BEC) in the regular CSLA to achieve lower area and increased speed of operation. This logic is replaced in RCA with "Cin=1". This logic can be implemented for different bits which are used in the modified design. The main advantage of this BEC logic comes from the fact that it uses lesser number of logic gates than the n-bit Full Adder (FA) structure. As stated above the main idea of this work is to use BEC instead of the RCA with "Cin=1" in order to reduce the area and increase the speed of operation in the regular CSLA to obtain modified CSLA. To replace the n-bit RCA, an (n+1) bit BEC logic is required. The structure and the function table of a 4-bit BEC are shown in Fig. 3 and Table I, respectively.

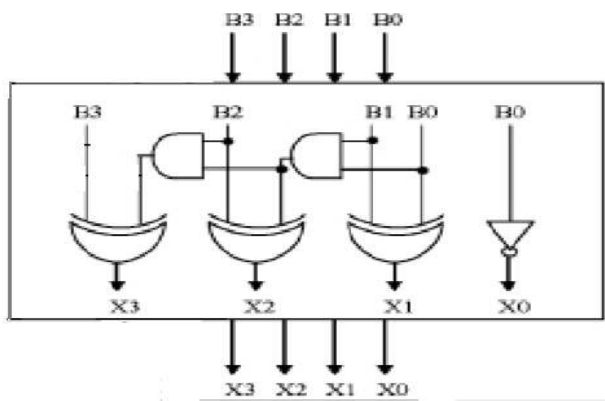


Fig. 3. 4-bit Binary to Excess-1 Converter (BEC).

B[4:0]	X[4:0]
0000	0001
0001	0010
⋮	⋮
1111	0000

TABLE I. FUNCTIONAL TABLE OF 4-BIT BEC

The Boolean expressions for the 4-bit BEC logic are expressed below.

$$\begin{aligned}
 X0 &= \sim B0 \\
 X1 &= B0 \wedge B1 \\
 X2 &= B2 \wedge (B0 \& B1) \\
 X3 &= B3 \wedge (B0 \& B1 \& B2)
 \end{aligned}$$

## Carry Select Adder

The CSLA is used in many computational systems design to moderate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. It uses independent ripple carry adders (for Cin=0 and Cin=1) to generate the resultant sum. However, the Regular CSLA(RCSLA) is not area and speed efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input. The final sum and carry are selected by the multiplexers (mux). Due to the use of two independent RCA the area will increase which leads an increase in delay. To overcome the above problem, the basic idea of the proposed work is to use n-bit binary to excess-1 code converters (BEC) to improve the speed of addition. This logic can be replaced in RCA for "Cin=1" to further improves the speed and thus reduces the delay. Using Binary to Excess-1 Converter (BEC) instead of RCA in the RCSLA will achieve lower area, delay which speeds up the addition operation of Modified CSLA (MCSLA)[4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure because the number of gates used will be decreased.

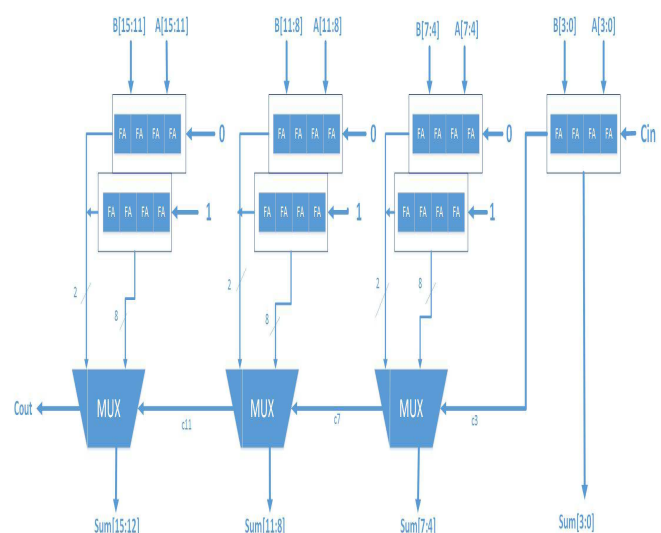


Fig. 4. 16-bit Uniform Regular Carry Select Adder (URCSLA).

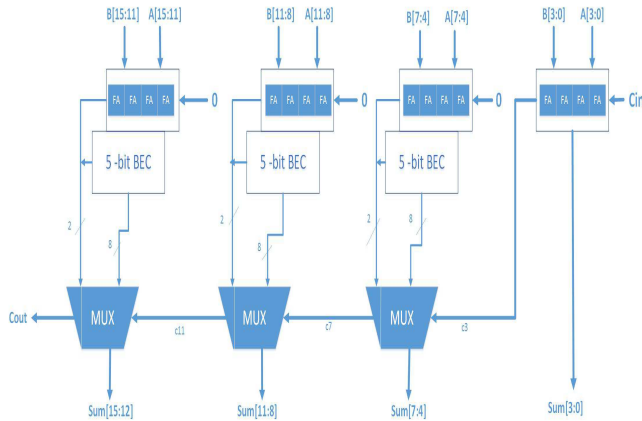


Fig. 5. 16-bit Uniform Modified Carry Select Adder (URCSLA).

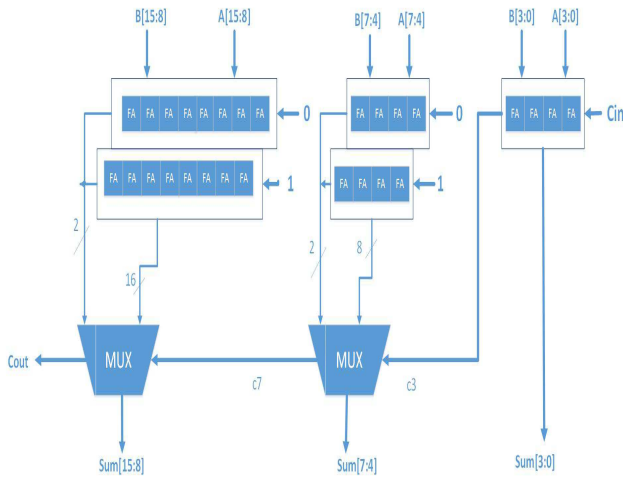


Fig. 6. 16-bit Variable Regular Carry Select Adder (URCSLA).

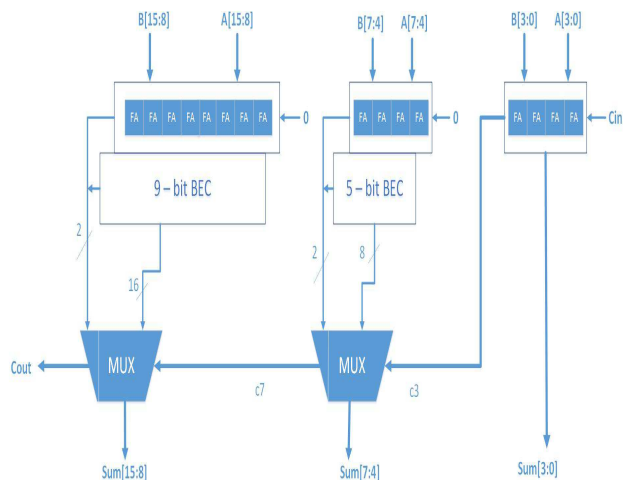


Fig. 7. 16-bit Variable Modified Carry Select Adder (URCSLA).

(VCSLA) block size is variable. The delay at "Cin" input stage can be reduced using variable type of CSLA. Theoretically, delay and area of CSLA are  $O(\sqrt{n})$  and  $O(2n)$  respectively.

The 16-bit Regular CSLA architecture is uniform block size (URCSLA) consists of 4-bit RCA and multiplexers as shown in figure 4. The 16-bit Modified CSLA (UMCSLA) similar to 16-bit URCSLA in which RCA with "Cin=1" is replaced by BEC at each stages. The 16-bit Variable size Regular CSLA (VRCSLA) also similar to URCSLA but at each stages the RCA block is variable as 4, 4, 8 sizes cascaded as shown in Fig. 6. The only difference in 16-bit Variable Modified CSLA (VMCSLA) is RCA with "Cin=1" is replaced by BEC. For 4-bit RCA, 5-bit BEC is used, and for 8-bit 9-bit BEC is used as shown in Fig. 7.

Similarly, a 32 and 64-bit of Regular and Modified CSLA can also be developed in two modes of different block sizes.

### III. KOGGE STONE ADDER

The Kogge-Stone Adder is the fastest parallel prefix adders[5][6] are obtained from Carry Look Ahead (CLA) structure with focus on design time and is the common choice for high performance adders in industry. The parallel-prefix adder becomes more favorable in terms of speed due to the  $O(\log 2n)$  delay through the carry path compared to  $O(n)$  for the RCA. The arrangement of the prefix network specifies the type of the Parallel Prefix Adder. This comes at the cost of long wires that must be routed between stages. The tree also contains more PG cells; while this may not impact the area if the adder layout is on a regular grid, it will increase power consumption. Despite these cost, KSA is generally used for wide adders because it shows the lowest delay among other structures.

The complete functioning of KSA can be easily comprehended by analyzing it in terms of three distinct stages:

1. Pre-processing stage
2. Carry generation network
3. Post processing stage

#### Pre-Processing Stage

In this stage, generate and propagate signals to each pair of inputs A and B are computed. These signals are given by the logic equations 1 & 2:

$$P_i = A_i \text{ xor } B_i \quad (1)$$

$$G_i = A_i \text{ and } B_i \quad (2)$$

#### Carry Generation Network

In this stage, carries corresponding to each bit is computed. Execution of these operations is carried out in parallel[5].

A 16-bit carry select adder can be developed in two different sizes namely Uniform block size and Variable block size. In Uniform Carry Select Adder (UCSLA), each block size is fixed in all stages, but in Variable Carry Select Adder

After the computation of carries in parallel they are segmented into smaller pieces. It uses carry propagate and generate as intermediate signals which are given by the logic equations 3 & 4:

$$P_{i:j} = P_{i:k+1} \text{ and } P_{k:j} \quad (3)$$

$$G_{i:j} = G_{i:k+1} \text{ or } (P_{i:k+1} \text{ and } G_{k:j}) \quad (4)$$

## Post-Processing Stage

This is the final step to compute the summation of input bits. It is common for all adders and the sum bits are computed by logic equations 5 & 6:

$$C_{i-1} = (P_i \text{ and } C_{in}) \text{ or } G_i \quad (5)$$

$$S_i = P_i \text{ xor } C_{i-1} \quad (6)$$

The 8-bit Kogge- Stone Adder(KSA) will be explained in detail below. An 8-bit KSA is built from eight generate and propagate (GP) blocks, eight black cells (BC) blocks, eight gray cell (GC) blocks, and nine sum blocks as shown in the Fig. 12. The details of the various blocks used in the structure of KSA are shown below.



Fig. 8. GP Block

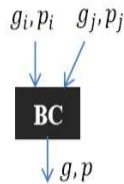


Fig. 9. BC Block

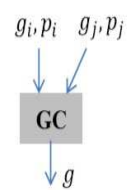


Fig. 10. GC Block

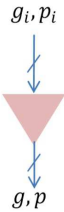


Fig. 11. Buffer

The Kogge-Stone Adder(KSA) is widely used in high-performance 32-bit, 64-bit, and above adders as it reduces the critical path to a great extent compared to the ripple carry adder.

## IV. PROPOSED CSLA

The Proposed CSLA architectures(PCSLA) is similar to 16-bit Regular and Modified CSLA in both uniform and variable block sizes.. The Only change in Proposed CSLA(PCSLA) is that Kogge Stone Adder is used instead of RCA. Similarly, the 32-bit and 64-bit Proposed CSLA architectures is designed as shown in Figures 17 & 18.

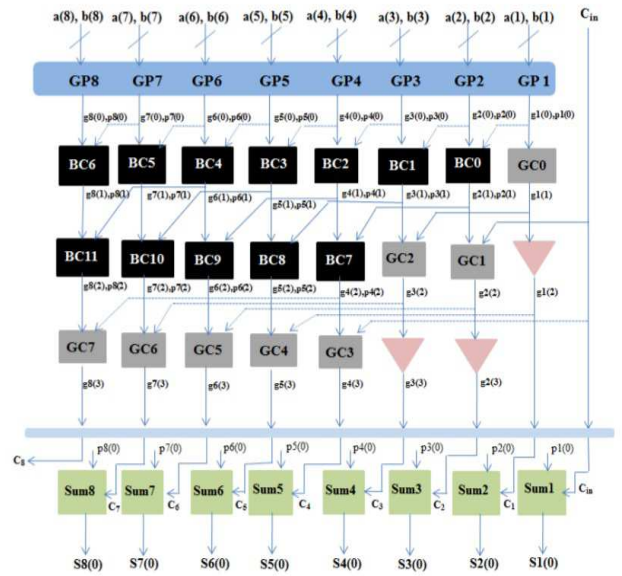


Fig. 12. 8-bit Kogge Stone Adder (KSA)

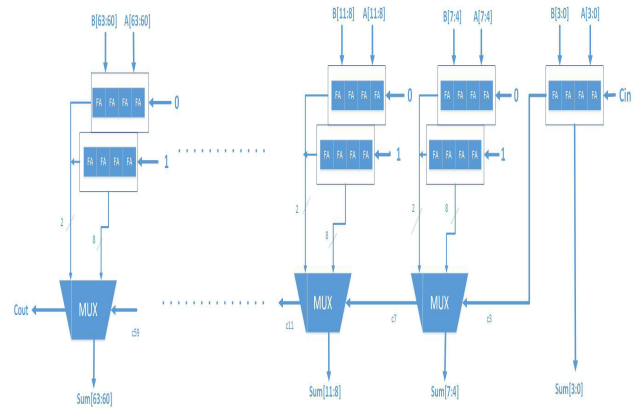


Fig. 13. 64-bit Uniform Regular Carry Select Adder (URCSLA).

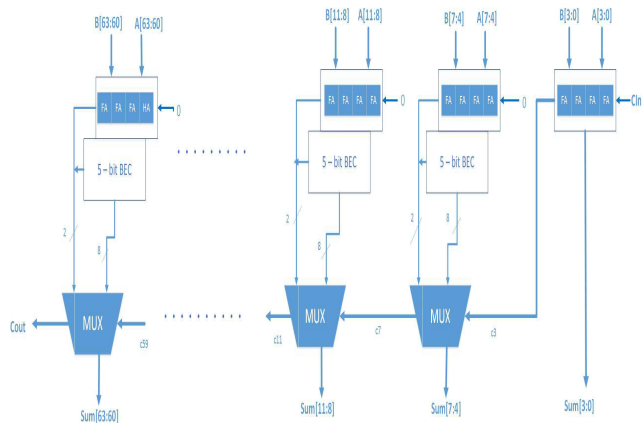


Fig. 14. 64-bit Uniform Modified Carry Select Adder (UMCSLA).

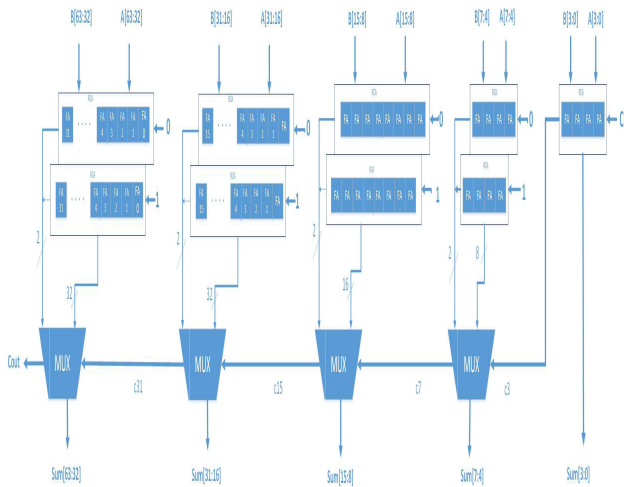


Fig. 15. 64-bit Variable Regular Carry Select Adder (VRCSLA).

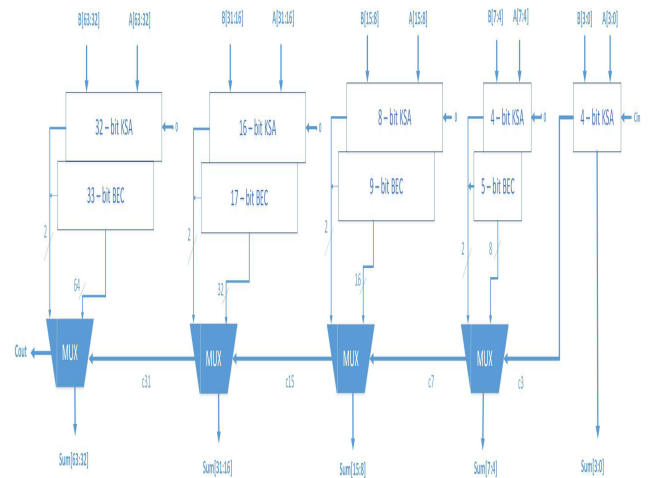


Fig. 18. 64-bit Variable Proposed Carry Select Adder (VPCSLA).

## V. IMPLEMENTATION RESULTS

The Regular, Modified and Proposed Carry Select Adders were designed using Verilog language in Xilinx ISE Navigator 14.2 and all the simulations are performed using Xilinx ISE simulator. The performance of Proposed CSLA (PCSLA) is analyzed and compared against the Regular and Modified CSLA designs in different modes of block sizes i.e., Uniform and Variable block size.. In this Proposed CSLA architecture, the implementation code for 4, 8, 16 and 32-bit Kogge- Stone Adders(KSA) were developed and corresponding values of logic and route delay were tracked. These values are compared to 4, 8, 16 and 32-bit Ripple Carry Adders logic and route delay. Table II shows the comparison of Regular CSLA with Ripple Carry Adders(RCSLA), Modified CSLA with BEC (MCSLA) and Proposed CSLA with KSA(PCSLA) with in terms of logic and route delay for Uniform and Variable block size. The simulated output of 64-bit Proposed CSLA shown in Fig. 20.

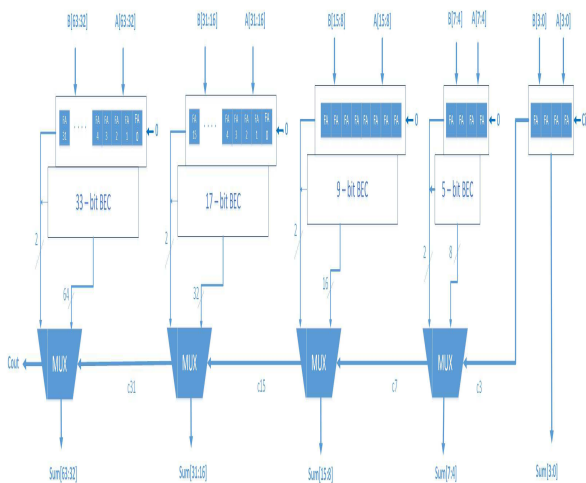


Fig. 16. 64-bit Variable Modified Carry Select Adder (VMCSLA).

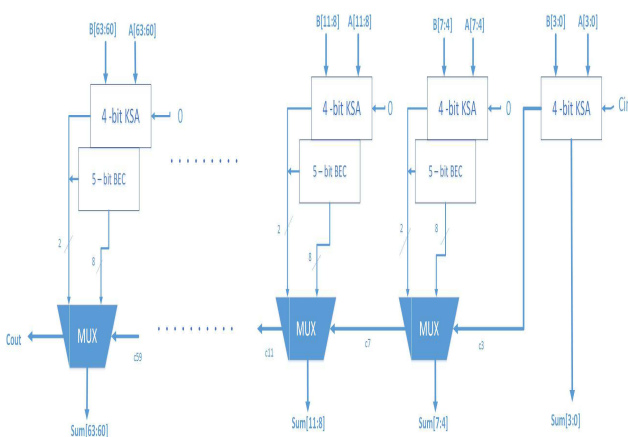


Fig. 17. 64-bit Uniform Proposed Carry Select Adder (UPCSLA).

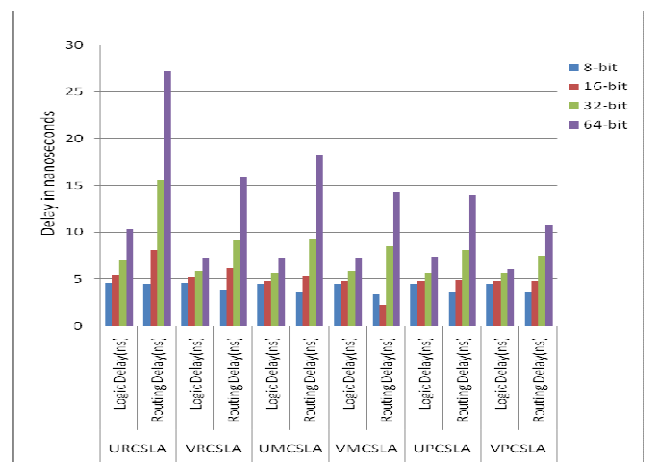


Fig. 19. Delay (logic and routing) comparison between different CSLA architectures.

CSLA Adder Type		Total Delay (ns)	Logic Delay (ns)	Routing Delay (ns)
URCSLA	8-bit	8.937	4.609	4.411
	16-bit	13.502	5.425	8.077
	32-bit	22.632	7.057	15.575
	64-bit	37.532	10.321	27.211
UMCSLA	8-bit	7.953	4.402	3.551
	16-bit	10.166	4.808	5.358
	32-bit	14.943	5.620	9.323
	64-bit	25.504	7.244	18.260
UPCSLA	8-bit	7.932	4.402	3.530
	16-bit	9.704	4.810	4.894
	32-bit	14.056	5.622	8.134
	64-bit	21.253	7.272	13.981
VRCSLA	8-bit	8.411	4.605	3.806
	16-bit	11.388	5.226	6.162
	32-bit	15.463	5.835	9.203
	64-bit	23.134	7.246	15.888
VMCSLA	8-bit	7.787	4.462	3.383
	16-bit	10.098	4.812	5.286
	32-bit	14.301	5.828	8.478
	64-bit	21.554	7.244	14.310
VPCSLA	16-bit	9.620	4.812	4.808
	32-bit	13.097	5.634	7.463
	64-bit	16.756	6.036	10.720

TABLE II. COMPARISON OF RCSLA, MCSLA AND PCSLA IN UNIFORM AND VARIABLE BLOCK SIZE.

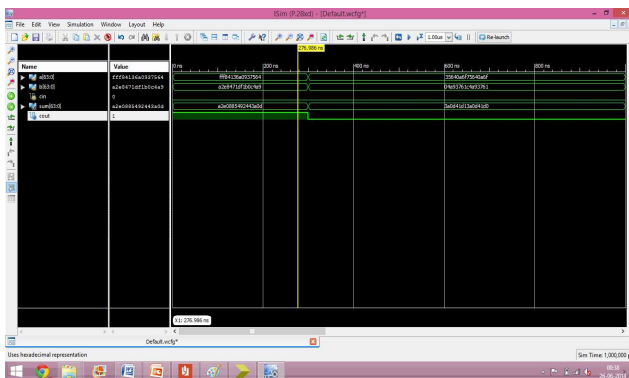


Fig. 20. Simulation Output of 64-bit Proposed CSLA.

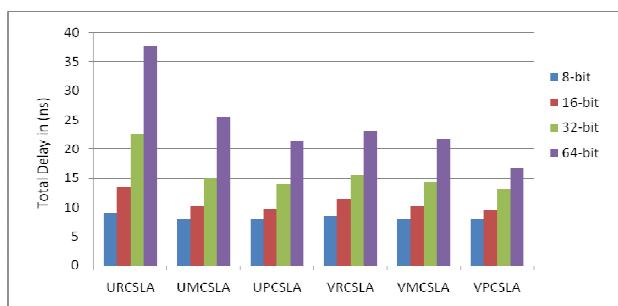


Fig. 21. Total Maximum Combinational Delay comparison between different CSLA architectures.

## VI. CONCLUSION

The Proposed High Speed CSLA in this paper is to reduce the delay of Modified CSLA(MCSLA). The replacement of Parallel -Prefix Adders(KSA) in place of Ripple Carry Adders offers great advantage in the reduction of delay. And the Proposed CSLA architecture also compared with Uniform and Variable Block Size. The compared result shows that the Proposed CSLA greatly reduces delay. The Proposed CSLA architecture is therefore, faster because of less delay and area efficient for VLSI hardware implementations. It would be interesting to investigate the design of 128-bit bit Proposed CSLA in both Uniform and Variable block size.

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