International Journal of Ethics in Engineering & Management Education
Website: www.ijeee.in (ISSN: 2348-4748, Volume 1, Issue 4, April 2014)

Design of Reliable Router Architecture Using Hamming Code Error Correction Techniques

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***Abstract*— In this project, a new reliable Network on Chip suitable for dynamically reconfigurable Multiprocessors on Chip systems is designed and simulated. The proposed NoC design is based on routers performing online error detection of routing algorithm and data packet errors. This project focuses on adaptive routing algorithms which allow bypassing faulty components or processor elements dynamically implemented inside the network. The proposed routing error detection mechanism helps distinguish routing errors from bypasses of faulty components.. The primary uniqueness in this NoC approach is that only the permanently faulty parts of the routers are disconnected. Hence, this technique results in high run time throughput in the NoC without data packet loss due to the self-loopback mechanism inside each router.**

I. INTRODUCTION

The trend of embedded systems has been moving toward multiprocessor systems-on-chip (MPSoCs) in order to meet the requirements of real-time applications. The complexity of these SoCs is increasing and the communication medium is becoming a major issue of the MPSoC .Integrating a network-on-chip (NoC) into the SoC provides an effective means to interconnect several processor elements or intellectual properties .The NoC medium features a high level of modularity, flexibility, and throughput. A NoC comprises routers and interconnections allowing communication between the PEs and/or IPs. The NoC relies on data packet exchange. The path for a data packet between a source and a destination through the routers is defined by the routing algorithm. Therefore, the path that a data packet is allowed to take in the network depends mainly on the adaptiveness permitted by the routing algorithm (partially or fully adaptive routing algorithm), which is applied locally in each router being crossed and to each data packet.

Dynamically reconfigurable 2-D mesh NoCs are suitable for field programmable gate array (FPGA)-based systems. For achieving a reconfigurable NoC, an efficient dynamic routing algorithm is required for the data packets. It should provide high NoC performance in terms of throughput while preserving flexibility and reliability. This paper describes a new reliable dynamic NoC which is a mesh structure of routers that are able to detect routing errors for adaptive routing based on the *XY* algorithm. This approach includes data packet error detection and correction with Hamming codes. The originality of the proposed architecture is its ability to localize accurately error sources, allowing the throughput and network load of the NoC to be maintained. The considered routing algorithm is based on the adaptive turn model routing scheme and the well known *XY* algorithm. This adaptive algorithm is livelock- and deadlock-free and allows data packets to pass around faulty regions.

II. ARCHITECTURE OF THE SWITCH

The switch has four directions (North, South, East, West) suitable for a 2-D mesh NoC. The PEs and IPs can be connected directly to any side of a router. Therefore, there is no specific connection port for a PE or IP. The proposed detection mechanisms can also be applied to NoCs using five port routers with a local port dedicated to an IP. Each port direction is composed of two unidirectional data buses (input and output ports). Each input port is associated to a first-input, first-output (FIFO) (buffers) and a routing logic block. The switch operation is based on the store-and-forward switching technique. This technique is suitable for dynamically reconfigurable NoC. The data flow control used in our architecture is the Ack/Nack solution, which can handle fault-tolerant transmissions. This solution relies on the retransmission of packets being received as faulty by a neighboring node. If a neighboring router receives a flit containing an error that cannot be corrected by the ECC, a Nack is sent back and the whole packet is retransmitted. Otherwise, an Ack is generated at full packet reception. More precisely, an Ack is generated only when all the flits of the data packet have been received and checked by the router, which reduces latency. The Hamming ECC is considered for switch, in order to provide a convenient tradeoff between area overhead and error correction capacity. This choice permits the correction of single event upset (SEU) errors (one bit flip in a flit) and the detection of multiple event upset (MEU) errors (two bit flips in a flit). Moreover, the Hamming code is more suitable for NoCs based on Ack/Nack flow control than the parity bit check. Indeed, on a single bit-flip error occurrence, error correction is possible with the Hamming ECC, whereas the single parity check would require packet retransmission and hence an increased transmission latency.

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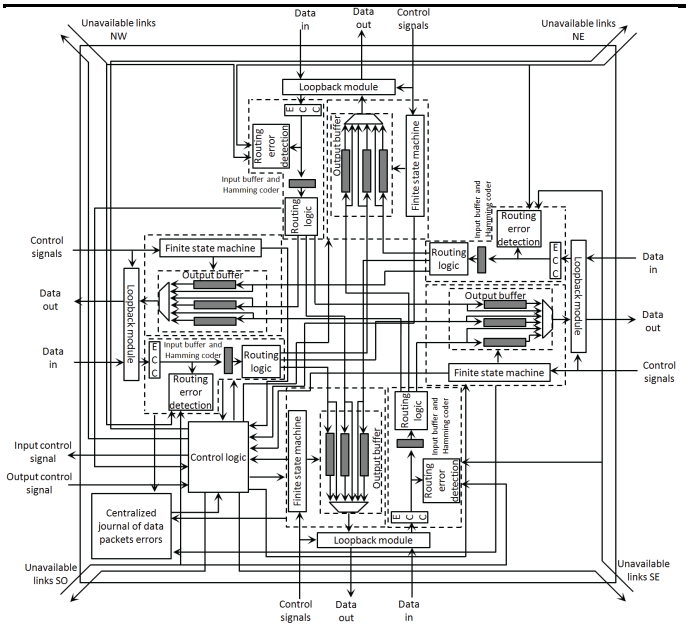
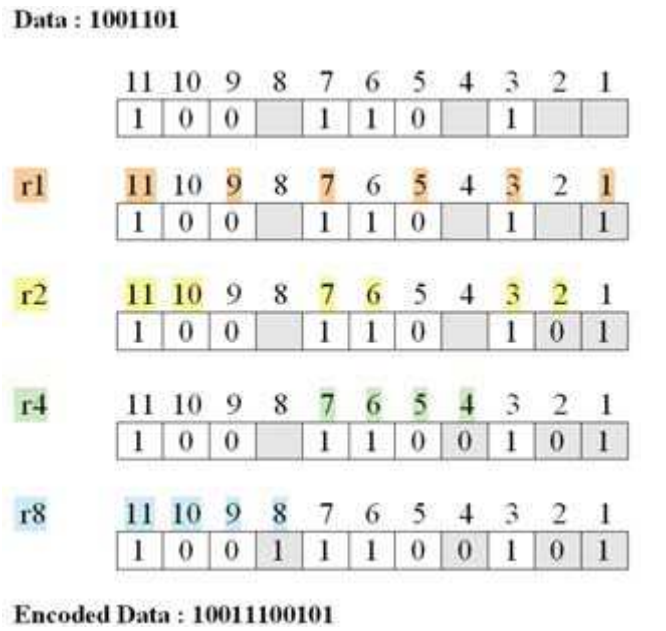
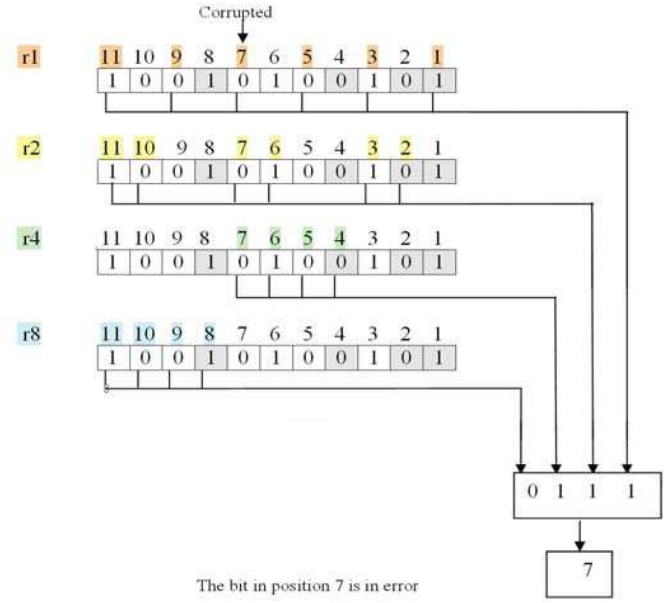


Fig 1. Architecture of the reliable switch





Designing (n, k, t) Hamming code

Forward error-correction coding also known as 'channel coding' is a type of digital signal processing that improves reliability of the data by introducing a known structure into the data sequence prior to transmission. As the name suggests, this coding technique enables the decoder to correct errors without requesting retransmission of the original information. Hamming code is a typical example of forward error correction. In a communication system that employs forward error-correction coding, the digital information source sends a data sequence to an encoder. The encoder inserts redundant (or parity) bits, thereby outputting a longer sequence of code bits, called a 'code word.' These code words can then be transmitted to a receiver, which uses a suitable decoder to extract the original sequence. The (n, k, t) code refers to an 'n'-bit code word having 'k' data bits (where n > k) and 'r' (=n–k) error-control bits called 'redundant' or 'redundancy' bits with the code having the capability of correcting 't' bits in the error (i.e., 't'corrupted bits).If the total number of bits in a transmittable unit (i.e., code word) is'n' (=k+r), 'r' must be able to indicate at least 'n+1' (=k+r+1) different states.

For example, a 7-bit ASCII code requires four redundancy bits that can be added at the end of the data unit or interspersed with the original data bits to form the (11, 7, 1) Hamming code. These redundancy bits are placed in positions 1, 2, 4 and 8 (the positions in an 11-bit sequence that are powers of '2'). For clarity in the examples below, these bits are referred to as 'r1,' 'r2,' 'r4' and 'r8.'In the Hamming code, each 'r' bit is the parity bit for one combination of data bits as shown below:

r1: bits 1, 3, 5, 7, 9, 11
r2: bits 2, 3, 6, 7, 10, 11
r4: bits 4, 5, 6, 7
r8: bits 8, 9, 10, 11

Error detection and correction. Suppose that by the time the above transmission is received, the seventh bit has changed from '1' to '0.' The receiver takes the transmission and recalculates four new parity bits, using the same sets of bits used by the sender plus the relevant parity 'r' bit for each set. Then it assembles the new parity values into a binary number in the descending order of 'r' position (r8, r4, r2, r1). In the given example, this step gives us the binary number '0111' ('7' decimal), which is the precise location of the corrupted bit. Once the bit is identified, the receiver can complement its value and correct the error. The beauty of the technique is that it can be easily implemented in hardware and the code is corrected before the receiver knows about it.

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SYNTHESIS

The proposed architecture has been implemented in Xilinx Virtex -6 and the synthesis output waveform with the error detection done by hamming code is shown below.

CONCLUSION

With the use of these hamming codes, error detection becomes easier and reduces latency, thus increasing speed of packet transmission and making router reliable. So, we can accurately locate whether the data errors are on the data bus, the input port, or output port, and whether the faults are permanent or transient.

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