# Reducing glitches in 2MHz, 1.8V Buck Converter with ZVS technique in 180nm UMC technology

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*Abstract—* **This paper presents a deglitching circuit integration for zero-voltage switching (ZVS) PWM synchronous buck converter, which is designed to operate at low output voltage and high efficiency typically required for portable systems. The design of Buck Converter depicts switching losses. This is reduced by the soft switching technique, via, non-overlapping block before the driver stage to effectively increase the efficiency. Glitches occur at the output of driver stage and it is reduced by adding deglitching circuit before the switching power MOSFET stage. The suggested design modification ensures increased performance in the Buck converter**. **At the circuit level, implementation of the various blocks is done in CMOS 180nm, using UMC technology model file on the Cadence Virtuoso platform.**

*Index Terms—***Buck Converter, Zero-Voltage Switching (ZVS) Technique, Switching losses, Glitches, Deglitching circuit.**

## I.INTRODUCTION

A simple DC-DC switching converter circuits consists of two semiconductor switches, one inductor and one capacitor. The arrangement of the switches and storage elements defines the topology of the switching converter. Switching converter often requires complex control circuits, and electromagnetic interface (EMI) fillters. The one of the fundamental topology of switching converter is the BUCK Converter. The Buck converter converts the input DC to a lower DC output voltage level. The next generation of portable products, such as personal communicators and digital assistants, has demanded improvement in dc-dc converter topology in order to increase battery life time and enable smaller, cheaper systems. Since many portable devices operate in low-power standby modes for a majority of the time they are on, increasing light-load converter efficiency can significantly increase battery lifetime. A key element in this task, especially at low output voltages that future microprocessor and memory chips will need, is the synchronous rectifier.

  A synchronous rectifier is an electronic switch that improves power-conversion efficiency by placing a low resistance conduction path across the diode rectifier in a switch-mode regulator. MOSFETs usually serve this purpose. However, higher input voltages and lower output voltages have brought about very low duty cycles, increasing switching losses and decreasing conversion efficiency.[4] So in this paper, we have optimized the efficiency of the synchronous buck converter by

eliminating switching losses using soft switching technique called ZVS (zero Voltage Switching) and deglitching circuit. Section 2 illustrates the specification of the design and the working principle of Buck Converter. Section 3 discusses the Zero Voltage Switching (ZVS) technique which is used to design a non overlapping clock generator. Section 4 includes the explanation basic blocks of DC-DC down converter. Section 5 shows the design implementation of deglitching circuit in the main block of the Buck converter and simulation results of integrated circuit. Section 6 gives the conclusion and future work of the design approach used in the Buck converter.

## II.    SPECIFICATIONS OF THE DESIGN

This section consists of detailed specifications used for the design of 2MHz, 1.8V DC-DC down converter. The specifications are enlisted in Table. 1.

| Variable | Name | Value | Variation |
|---|---|---|---|
| Power Stage supply voltage | Vin | 3.3V | ±10 % |
| Core voltage | Vdd | 1.8V | ±10% |
| Reference voltage | Vref | 1.1V | ±2% |
| External Inductance | L | 2.275uH | ±30% |
| External Capacitance | C | 7uF | ±30% |
| Load current range | | | 0.2 to 0.6A |
| Output voltage variation | Vout | | ≤5% |
| Clock frequency | | | 2MHz |
| Temperature range | | | -40∘C to 125∘C |
| Technology | UMC180 | | |
| Tool | Cadence | | |

Table. 1: Specifications of DC-DC Converter

*Basic Working Principle of DC-DC Converter*
Basic principle of DC-DC Converter is explained in following section and basic buck topology is shown in Fig. 1, When the switch is in position one, output voltage is equal to the input voltage and when the switch is in position two, the output voltage is equal to zero [2][4]. The resulting average voltage

level at the output is a function of the time when the switch is in position one and two respectively.

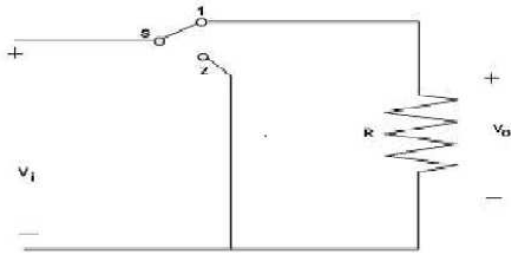This function is called duty ratio and it is defined by the expression,

$D = Vo/Vin$



Fig.1: Basic Buck Topology

Where,

Vo = average output voltage.

Vin = DC voltage generated by the power source.

The main problem of this basic circuit is the voltage ripple of the output signal of the converter. For this reason a LC-filter is used to decrease the voltage ripple. This modified circuit is shown in Fig. 2.
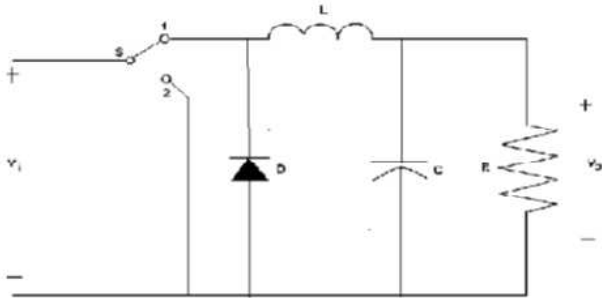


Fig. 2: Modified Buck Topology

Since the average current through the load resistor R is approximately the same as the average current of the inductor, the voltage Vo across the load resistor contains less ripple. A diode is used when the switch is in position two. This allows the capacitor to be charged in both switching positions. When the switch is in position one the energy is transferred from the power source to the capacitor and when the switch is in position two the capacitor is charged with the energy stored in the inductor. This type of operation results in high power efficiency for buck converter.

III. ZVS TECHNIQUE (ZERO VOLTAGE SWITCHING)

The following section discusses the Zero Voltage Switching (ZVS) technique which is used to design a non overlapping clock generator. The non overlapping clock generator

produces non overlapping clock signals are helped in reducing switching losses.

Specifically means zero-voltage turn-on, i.e., the voltage across the device is reduced to zero before the current increases. The clock generator for producing non-overlapping clock signals can be realized with a simple circuit constructed of logic gates. Such a circuit is shown in Fig. 3 and waveforms are shown in Fig. 4.
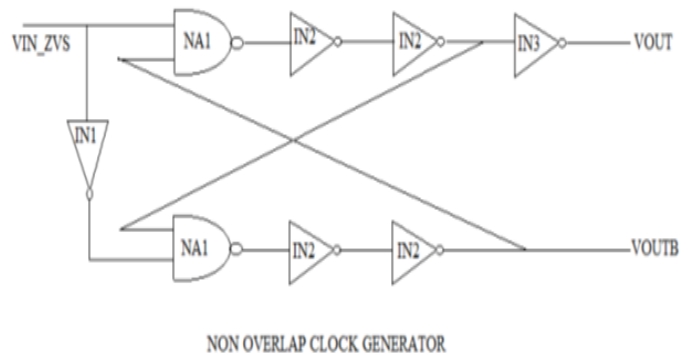

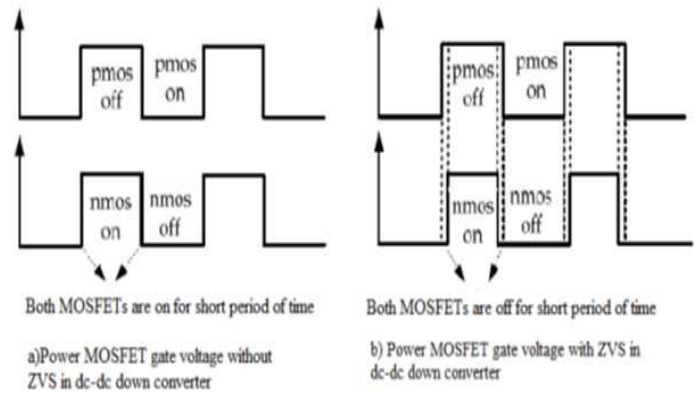
Fig. 3: Standard Non overlap clock generator



Fig. 4: Waveforms

*Non Overlap Clock Generator*

The PMOS power switch and NMOS power switch cannot be closed at the same time, or the voltage source will be shorted to ground, and generating current large enough to burn the transistors. To avoid the above situation, non-overlapping clocks are needed for driving the two power switches. Since the two power switches belong to different types (P-type and N-type), the clocks are not traditional non-overlapping signals with opposite phase, but are in-phase signals with different rising and falling edges.[5] The required clock waveforms are shown in Fig. 4.

The Fig. 5 shows the output waveforms of ideal non overlapping block for 2ns delay of inverters. In Fig. 5 first waveform is the input waveform for the ZVS block and it is

the output of comparator. The non overlap clock generator generates the in phase waveforms vout and voutb as shown in below figure. vout is applied to Nmos whose pulse width is lesser than voutb, so as to reduce the Nmos conduction for longer time otherwise most of the inductor current goes to ground.
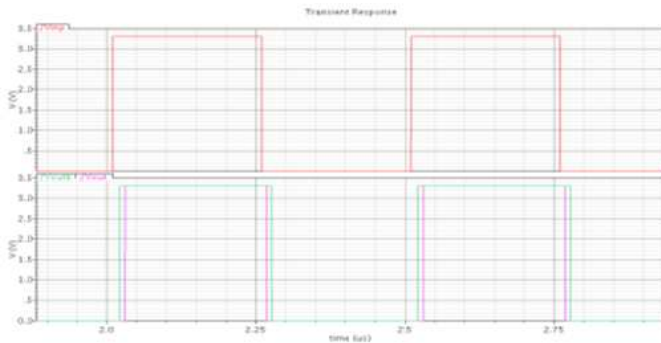


Fig. 5: Outputs of ideal non overlap block

## IV.BASIC BLOCKS OF DC-DC DOWN CONVERTER

This section includes the explanation basic blocks of DC-DC down converter that contribute to the closed loop system as shown in Fig. 6. Block consists of the modulator, the output filter, and the compensation network which closes the loop and stabilizes the system [2] [7].
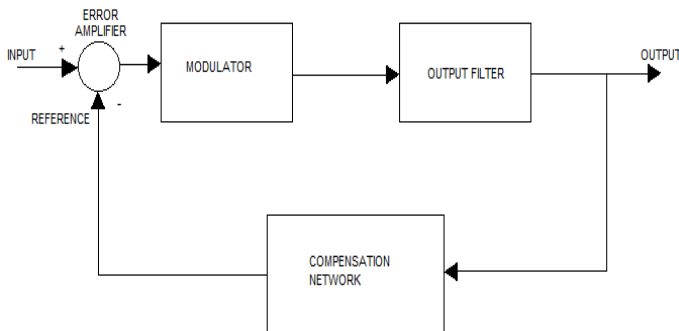


Fig. 6: Basic Blocks of Buck Converter

The input to the modulator is the output of the error amplifier, which is used to compare the output to the reference. The output of the modulator is the PHASE node. [2][7]There are many accurate models with which one can model this stage of the converter loop. Accurate and SSA models are also studied, but for the sake of simplicity we chose the average model, which simply linearizes the behavior of comparator and switching action. The output filter consists of the output inductor and all of the output capacitance. It is important to include the DC resistance (DCR) of the output inductor and the total Equivalent Series Resistance (ESR) of the output capacitor bank. The input to the output filter is the PHASE

node obtained from the modulator output and the output is fed to compensation network.

The feedback compensation design involves selection of a suitable compensation circuit configuration and positioning of its poles and zeros to yield an open loop transfer function [2]. Proper compensation of the system will allow for a predictable bandwidth with unconditional stability. In most cases, a Type II or Type III compensation network will properly compensate the system.

*Deglitching Circuit*
The following subsection includes the introduction about glitches, glitch causes and explanation of deglitching circuit is integrated with buck converter circuit to minimize the glitches occur at the output of the driver circuit.

The unwanted transitions are called glitches, which may occupy a considerable amount in the signal transition of a circuit [5]. Transient that leaves an initial state, enters the boundaries of another state for duration less than duration for state occurrence and returning to the initial state. Glitches are results in more power dissipation in the circuit. Glitch is also defined as pulse due to finite propagation time, when steady state analysis predicts no change in the sign.
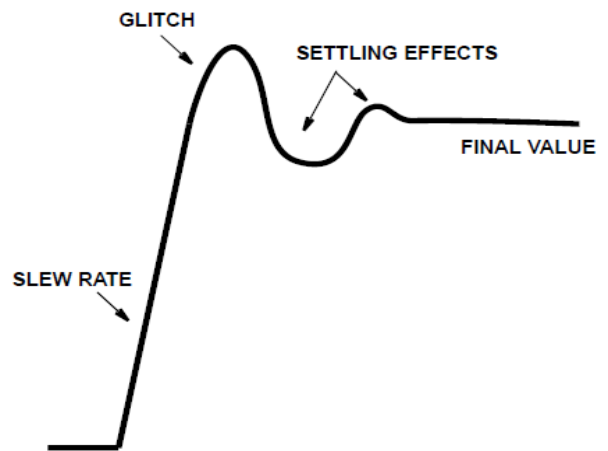


Fig. 7: Glitching Response

The above figure shows glitching response. The response contains glitch, and settling effects, that must die down in order to reach the new steady state output.

Glitch Area is the measure of the area under the first transient of the output of the D/A converter. The glitch is assumed to be triangular in shape and is calculated as shown in Fig. 9.The glitch is the first peak transient. Some manufacturers use the glitch 'doublet' theory where the specification given is a net glitch area. [5].
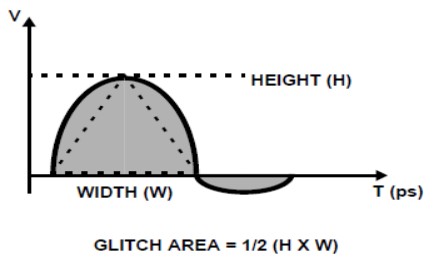
Fig. 8. Glitch Area

The glitch doublet sums the area of the initial glitch transient and the area of the settling effects. These areas are then added together to yield some very small unrealizable number by most board level designers.

The 'singlet' or peak glitch area is a more realistic specification for board and system level designers as they can more adequately evaluate the severity of the glitch.

Glitch causes

The glitch of a given circuit can limit the overall spectral performance of the converter and make it unusable.

Typically the switching time of inputs are asymmetrical, meaning that the turn off time is faster than the turn on time.

As shown in Fig. 9 [6] and Fig. 10[7], the new deglitching circuits can be built to reduce the effect of the glitches at the output of driver stage.
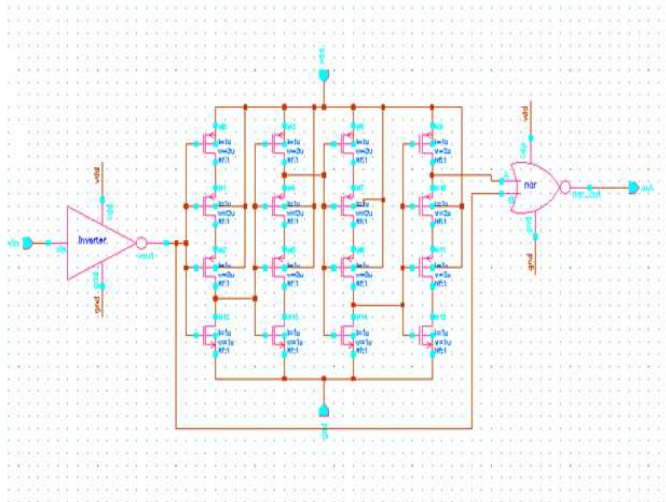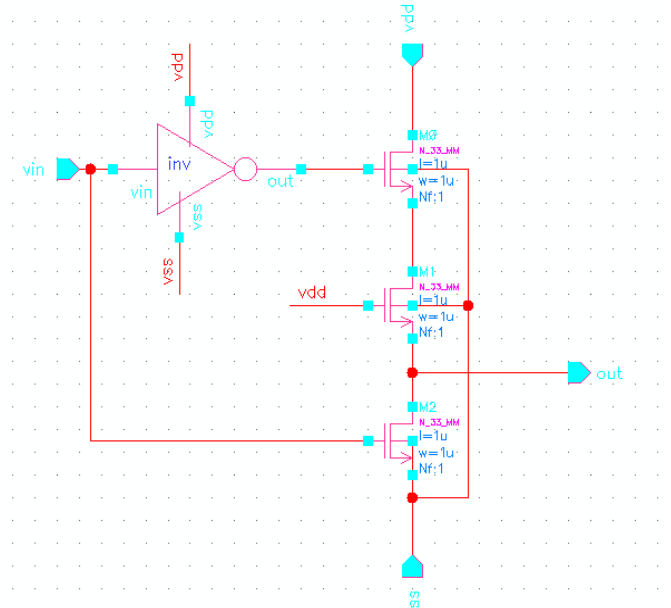


Fig. 9: Deglitching Circuit1



Fig. 10: Deglitching Circuit2

## V.IMPLEMENTATION

The implementation part includes, entire buck converter circuit integrated with deglitching circuit.

The block diagram consists of power MOSFET module, drivers, comparator, error amplifier, voltage divider, bias module, ramp generator, ZVS module, deglitching circuit. The entire Buck Converter schematic is shown in Fig. 11.
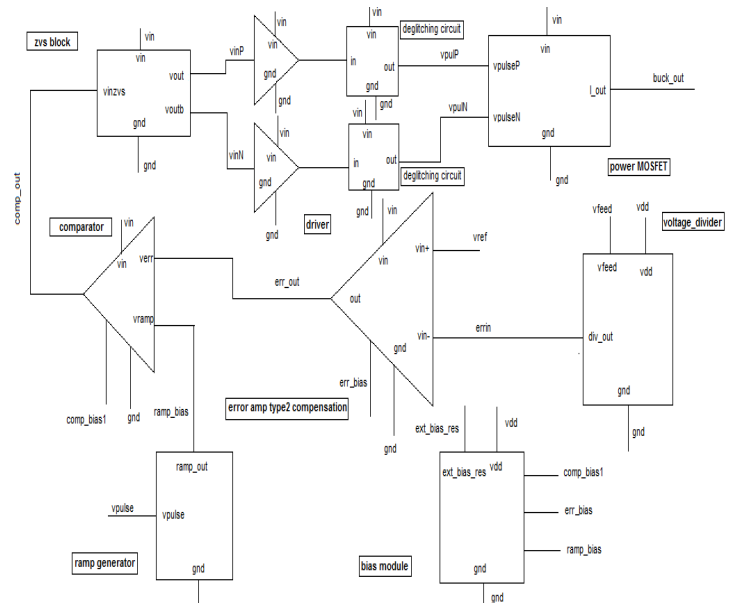


Fig. 11: Integrated Buck Converter circuit with deglitching circuit

Now the test circuit for buck converter is shown in Fig. 12. With this test circuit simulation is performed to see the functionality of the converter.
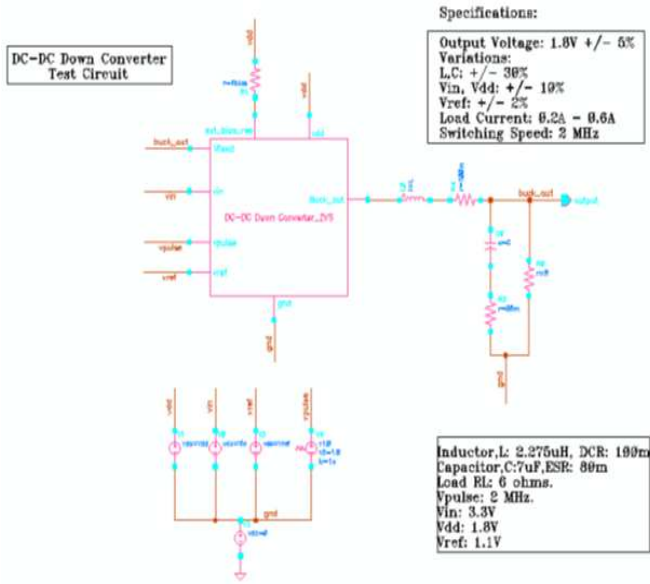


Fig.12: Test Circuit of DC-DC down Converter

## SIMULATION RESULTS

Simulation is done on designed Buck Converter. The entire test schematic of this design is shown in Fig. 12, which also includes external inductor and capacitor shown along with their parasitic resistors, ESR, DCR and load resistor.

Simulations results are obtained by considering load variation of 300mA at typical-typical process corner. Similarly results can be obtained with different load conditions as per the design specifications given in the Table. 1. The different corners of these simulations are specified as ss, snfp & fnsp for slow-slow, fast-fast, slowN-fastP, and fastN-slowP respectively, tt: being a typical-typical corner. So, once the simulations meets the requirements for a typical corner, it has to be repeated for all other process corners and RC variations.

Fig. 13 is the Transient response of buck converter circuit without deglitching circuit at load 300mA.It is seen from figure that output responds within 15uS and it settles around 1.83V.In this waveform we can observe more ripples. In this corner converter gives 87.91% efficiency.
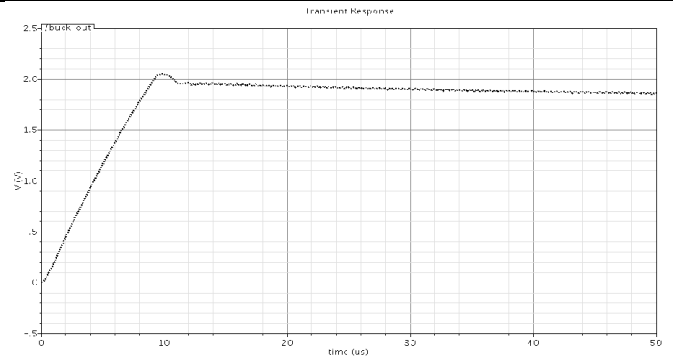


Fig.13: Transient response without deglitching circuit

Fig. 14 is the Transient response of buck converter circuit with deglitching circuit1 at load 300mA.It is seen from figure that output responds within15uS and it settles around 1.86V. In this waveform we can observe less ripples. In this corner converter gives 92.3% efficiency.
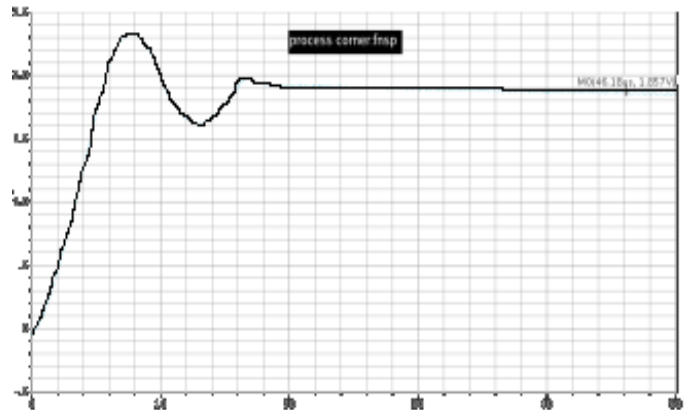


Fig.14: Transient response with deglitching circuit1

Fig. 15 is the Transient response of buck converter circuit without deglitching circuit at load 300mA.It is seen from figure that output responds within 15uS and it settles around 1.89V. In this corner converter gives 89.3% efficiency
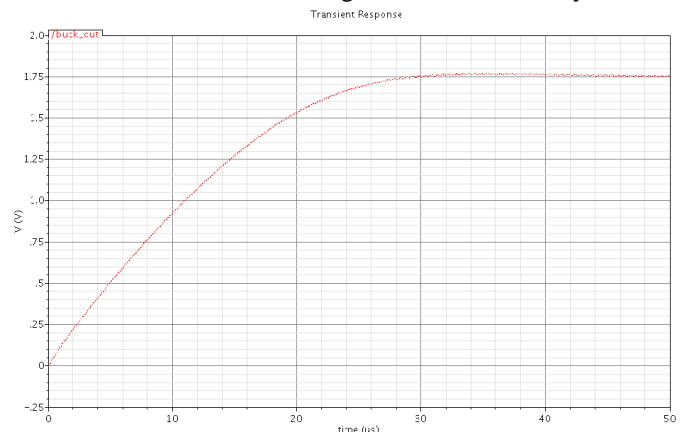


Fig.15: Transient response with deglitching circuit2

*Comparison of simulation Results*

Table.2 depicts the analysis of the DC-DC converter for its efficiency. The efficiency is calculated for 300mA load condition at typical process corner.

The below observation shows that the efficiency increases as output power increases. Hence the maximum efficiency is obtained with output power 579mW which is 92.3% for buck converter with deglitching circuit1 and minimum efficiency is obtained with output power 549mW which is 87.91% for the buck converter without deglitching circuit. Similarly efficiency is 89.3% for the buck converter with deglitching circuit2 with output power of 567mW.
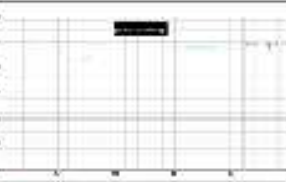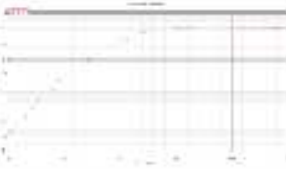
| Shematic | Simulation Result | Efficiency | Output Power |
|---|---|---|---|
| Without Deglitching Circuit | | 87.91% | 549mW |
| With Deglitching Circuit1 | | 92.3% | 579mW |
| With Deglitching Circuit2 | | 89.3% | 567mW |

Table. 2: Comparison of simulation Results

The below graph shows the output power variation for the buck converter at three different conditions such as without deglitching circuit, with deglitching circuit1 and with deglitching circuit2.
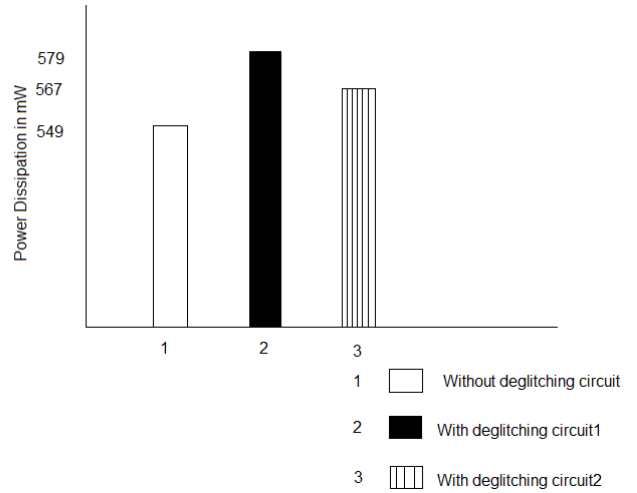


Fig. 16: Comparison Power Dissipation

Table. 3 consists of selection of input voltage for different process corners. Here worst case is slow-slow (ss), typical case is typical-typical (tt) and best case is fast-fast (ff). As per the design specs +/-10% variation is allowable for Vin. Hence the input voltages for tt, ss, ff, snfp and fnsp will be 3.3V, 3V, 3.6V, 3V, 3V are chosen respectively. It is observed that the maximum efficiency obtained at ff process corner is 93.9% and minimum efficiency obtained at ss process corner is 91.76%.

| Process corner | Input voltage | Input current | Output voltage | Output current | Efficiency |
|---|---|---|---|---|---|
| tt | 3.3V | 362.7mA | 1.86V | 300mA | 92.3% |
| ss | 3V | 403.2mA | 1.85V | 300mA | 91.76% |
| fnsp | 3V | 401.5mA | 1.858V | 300mA | 92.55% |
| ff | 3.6V | 330mA | 1.86V | 300mA | 93.9% |
| snfp | 3V | 399mA | 1.851V | 300mA | 92.73% |

Table. 3: Efficiency calculation at different process corners.

## VI. CONCLUSION AND FUTURE WORK

In this paper main objective is to reduce switching losses and glitches, it is achieved by implementing ZVS technique and Deglitching circuit. Zero Voltage Switching technique and deglitching circuit are implemented successfully in this paper. From the calculations and results, it is found that Buck Converter efficiency is improved and power MOSFET switching losses and glitches are reduced. In previous design power efficiency achieved was 87.91%. After implementation of Zero voltage switching and deglitching circuit, power

efficiency is reached to 92.1%. Hence because of ZVS, switching losses in power stage were reduced.

In future work, ripples can be further reduced by varying the width and length of deglitching circuit. Other types of deglitching circuits may use to get less ripples and more efficiency. As another future work the impact of power MOSFETs design used in the Buck Converter on the deglitching effect could be investigated. The motivation for these design approaches is basically to reduce the transistor area but still achieve good efficiency of the Buck Converter performance.

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