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FPGA IMPLEMENTATION OF OFDM SOFTWARE DEFINED RADIO WITH 8PSK MODEM

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***Abstract*: Orthogonal frequency division multiplexing is a modulation technology which is widely adopted in many new and emerging wired and wireless communication systems. Advantages of OFDM are high spectral efficiency , robustness against a inter carrier and inter symbol interference. .This paper presents the hardware implementation of SDR using Orthogonal Frequency Division Multiplexing (OFDM) with phase shift keying(8PSK) modulation and demodulation. Design of the radio on the reconfigurable platform makes it more flexible .The paper covers design of transmitter and receiver on the reconfigurable platform like FPGA. This paper covers VLSI coding for Orthogonal Frequency Division Multiplexing (OFDM), Phase Shift Keying (8PSK), Fast Fourier Transform (FFT) Algorithms and the optimized algorithm for Direct Digital Frequency Synthesis (DDFS). A digital frequency synthesizer with optimized time and area resources has been proposed for the SDR to compute the sine and cosine function using only two multiplexers , thus proving to be optimized in terms of area and speed. Verilog HDL code was used as a description language for mapping Algorithms in VLSI. Xilinx Spartan 3E XC3S250 Field Programmable Gate Array (FPGA) was chosen as a Hardware Platform for the System Implementation.**

***Key Words:* Software Defined Radio, Direct Digital Frequency Synthesis, Orthogonal Frequency Division Multiplexing, 8PSK Modem.**

1. INTRODUCTION

With the exponential growth in the ways and means by which people need to communicate - data communications, voice communications, video communications, broadcast messaging, command and control communications, emergency response communications, etc. - modifying radio devices easily and cost-effectively has become business critical. Software defined radio (SDR) technology brings the flexibility, cost efficiency and power to drive communications forward, with wide-reaching benefits realized by service providers and product developers through to end users. A number of definitions can be found to describe Software Defined Radio, also known as Software Radio or SDR. The Wireless Innovation Forum, working in collaboration with the Institute of Electrical and Electronic Engineers (IEEE) P1900.1 group, has worked to establish a definition of SDR that provides consistency and a clear overview of the technology and its associated benefits.

Simply put Software Defined Radio is defined as : "Radio in which some or all of the physical layer functions are software defined" *

A Software Defined Radio (SDR) can also be defined as a radio in which the receive digitization is performed at some stage downstream from the antenna, typically after wideband filtering, low noise amplification, and down conversion to a lower frequency in subsequent stages - with a reverse process occurring for the transmit digitization. In an SDR, Digital Signal Processing in flexible and reconfigurable functional blocks define the characteristics of the radio. As technology progresses, an SDR can move to an almost total Software Radio (SR), where the digitization is at (or very near to) the antenna and all of the processing required for the radio is performed by software residing in high-speed digital signal processing elements. Using DDFS, we can generate the high frequency carrier waves in digital domain and modulate the message on it, and then convert it to analog form using a digital to analog converter (DAC) before antenna. This is referred to be the digital up-conversion (DUC) [1][2]. The counter-part of digital up-converter, on the receiver end, is digital down converter (DDC). VLSI has been a key technology for mapping communication and signal processing algorithms in hardware. The DDFS includes Lookup Table based designs and Coordinate Rotation Digital Computer (CORDIC) based designs., CORDIC based approaches have been used for the generation of Sine and Cosine. Lookup Table based designs require huge ROMs for implementation and are declared to be area-hungry. On the other hand, CORDIC based techniques use iterative algorithms for the computation of Sine and Cosine functions and are computationally inefficient. Singleton [3] used basic trigonometric identities to compute the values of Sine and Cosine. Each sample of Sine and Cosine requires 4 multiplications and 2 additions. However, the modified design in [5] is even simpler and faster. It utilizes 2 adders and 2 multipliers to generate a sample of sine and cosine. This design is more and time efficient But the Architecture proposed by [5], has utilized registers being triggered on the positive and negative edges of the same clock. Such designs are not synthesizable on Field Programmable Gate Arrays (FPGA). So, in this work, a novel architecture has been proposed which generates the Sine and Cosine function using only two 10 bit multiplexers. The proposed architecture

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reduces the required hardware resources while realizing a synthesizable efficient design to improve signal to noise ratio.

2. METHODOLOGY

This work contains simulation and Verilog HDL implementation of OFDM based transmitter and receiver system. The transmitter first converts the input data from a serial stream to parallel sets. Each set of data contains one information bit for each carrier frequency. Then, parallel data are modulated to the orthogonal carrier frequencies. The IFFT converts the parallel data into time domain waveforms. Finally, these waveforms are combined to create a single time domain signal for transmission.. The receiver basically performs the inverse of the transmitter by first separating the data into parallel streams. The FFT converts the parallel data streams into frequency domain data. The data are now available in modulated form on the orthogonal carriers. Demodulation down-converts this information back to the baseband. Finally, the parallel data are converted back into a serial stream to recover the original signal. The overall block diagram of the system has been shown in Fig. 1.

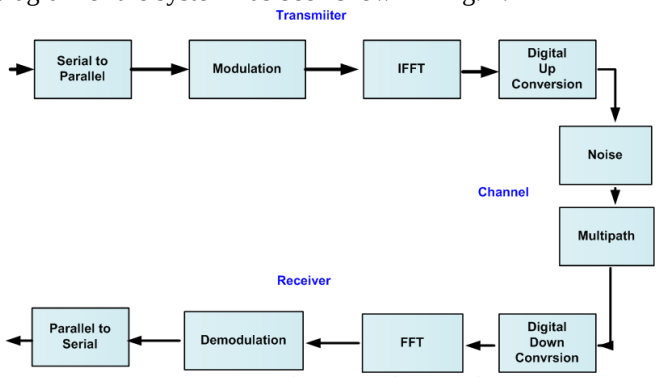

Fig. 1 Block Diagram of OFDM Software Defined Radio

3. BLOCK DIAGRAM AND IMPLEMENTATION

3.1. Serial-to-parallel Conversion and Parallel-to-Serial Conversion

The Serial-to-Parallel converter takes bits at a time and produces parallel streams of bits each. On the receiver end, the parallel-to-serial converter takes parallel streams, and transforms it into a stream of 8 bits serial data

.

3.2. Modulation and Demodulation

In this work, we have used 8 Phase Shift Keying (PSK) Modulation. The data is divided into chunks of a set of bits, each containing 3 bits of data, leading to 8 distinct combinations. Each combination is assigned as shown in Table I and Table II shows the mapping sequence and nodulation angle for QPSK Scheme. In order to ensure maximum likelihood, the separation between angles should be as large as possible. Hence, an angle assigned to each symbol is 22.5^0 67.5^0 ,112.5^0 ,157.5^0 ,202.5^0, 247.5^0,292.5^0 and 337.5^0

TABLE I.
CORRESPONDING ANGLE OF 8PSK MODULATION

Bit sequence	Modulation angle	Mapped sequence
000	π/8	.92+j.38
001	3π/8	.38+j.92
010	5π/8	-.38+j.92
011	7π/8	-.92+.j38
100	9π/8	-.92-j.38
101	11π/8	-.38-j.92
110	13 π /8	.38-j.92
111	15 π /8	.92-j.38

TABLE II.
ANGLE OF 4PSK(QPSK) MODULATION

Bit sequence	Modulation angle	Mapped sequence
00	π/4	+1+ j
01	3π/4	-1+ j
10	5π/4	-1- j
11	7π/4	+1- j

3.3. IFFT and FFT.

The IFFT and FFT [8][9] are the most time consuming part of the base-band OFDM processing for transmitter and receiver, respectively. Note that the IFFT operation can be performed using the FFT operation depicted in Fig. 3. By swapping the real and imaginary parts of the input sequence and swapping the real and imaginary parts of the output sequence, the FFT function is employed for the IFFT computation. Hence, if the OFDM transceiver is operated in time division multiplexing (TDM) mode, there is no additional hardware or software required for using the OFDM transmitter and receiver separately. In other words, one DSP should be able to handle both IFFT and FFT operations if its throughput is fast enough. Due to the simplicity, the radix-2, decimation-in-time FFT algorithm is chosen, implemented, and used for both IFFT and FFT operation at the transmitter and receiver, respectively. The "butterfly" is the smallest computational unit and implemented by Verilog HDL code.

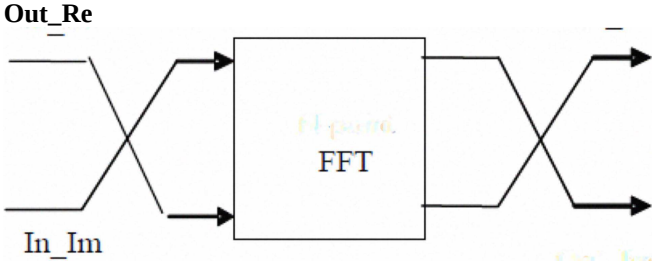

Fig. 2: The FFT operation of IFFT

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3.4 DIRECT DIGITAL FREQUENCY SYNTHESIS

The DUC is a digital circuit which implements the conversion of a complex digital baseband signal to a real pass band signal. The input complex baseband signal is sampled at a relatively low sampling rate, typically the digital modulation symbol rate. The Digital Down Converter (DDC) is the counter-part on the receiver end. The detailed description on DUC and DDC can be found in [6] [7]. This section focuses on the efficient hardware implementation of DDFS, which is backbone of the DUC and DDC The architecture for DDFS is shown in fig 3 uses. This architecture utilizes two adders, two multiplexers, two multipliers and two registers. A n optimized architecture uses only multiplexers for the calculation of sine and cosune function which is shown in fig 2.compared to the architecture proposed in [4], the required number of registers has been reduced. Depending upon the number of bits used, it results in considerable reduction of hardware resources.

4. EXPERIMETAL RESULTS

TABLE III

COMPONENTS USED COMPARISON

COMPONENTS	**Existing DDS architecture**	**Optimized DDS architecture**
No of multiplexer	2	2
No of multiplier	2	Nil
No of resister	2	Nil
No of adder/ substractor.	2	Nil

TABLE IV

TIMING ANALYSIS COMPARISON

Delay	**Existing DDS architecture**	**Optimized DDS architecture**
Combinational delay	7.762ns	7.602ns
Total delay	11.917ns	7.602ns

TABLE V

MEMORY ANALYSIS

Memory used	**Existing DDS architecture**	**Optimized DDS architecture**
	142840 kilobytes	132600 kilobytes

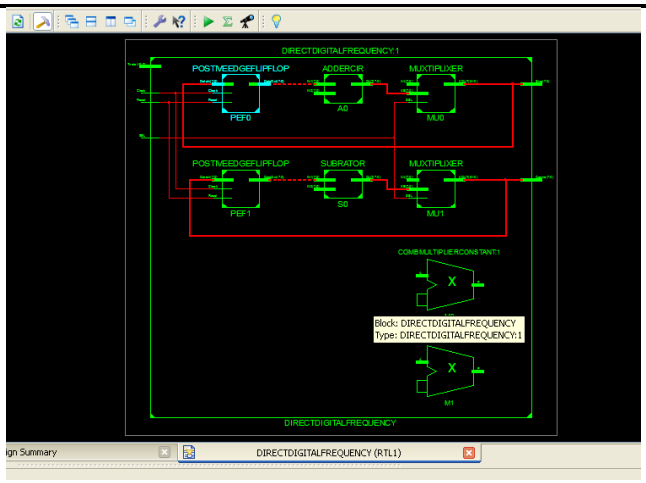

Fig 3.Optimised DDS Architecture

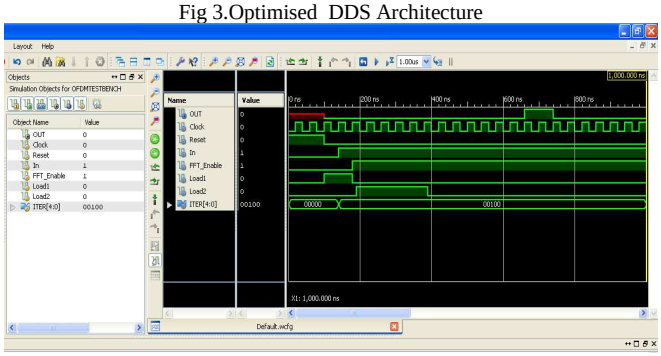

Fig 4.Existing DDS Architecture

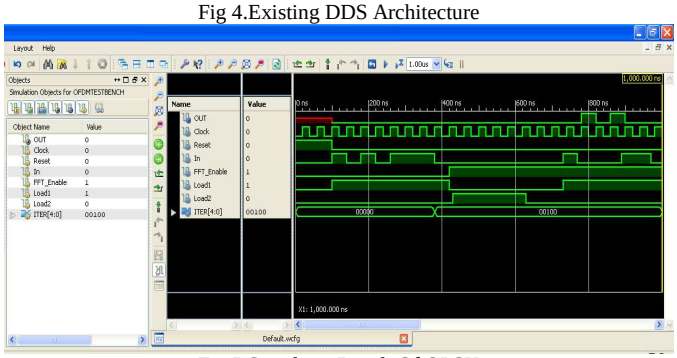

Fig 5.Simultion Result Of QPSK

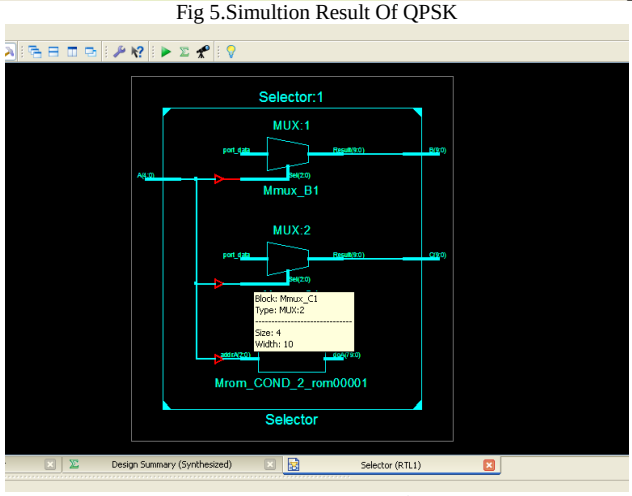

Fig 6.Simulation Result Of 8psk

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5. CONCLUSIONS

This paper presents a SDR system using OFDM transceiver. Both QPSK and 8PSK operational modes of the OFDM systems is discussed.PSK modulation is applied to this system to increase the signal to noise ratio. While still being able to provide high data rate. The framework consumes lesser silicon area and is realizable on FPGA.. The required memory resources are extremely less as only two 10 bit multiplexer have been used in the architecture Addditionally ,differences and similarities in data carrying capabilities between QPSK- and 8PSK of OFDM systems and the associated clock cycles required to demodulate data using FFT programming methods are provided Higher execution speed is achieved by using this method. The trade off of this optimization is a larger program memory requirement of veri log code.

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