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HEADFIRST SLIDING ROUTING FOR 3-D CHIP MULTIPROCESSORS

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***Abstract*—Long interconnects are becoming an increasingly important problem from both power and performance .The Headfirst sliding routing scheme to overcome the too much delay problem in simple TDMA-based vertical buses. Each vertical bus gives permission to communication time-slot for different chips at the same time periodically, which means these buses work with different phases. To avoid deadlocks, two VCs are required for all the routers. The main contribution of this paper is reduce the area, power and delay in the NOC chip by using 3D router with additionally gives Headfirst Sliding Routing. Network simulations show that Headfirst sliding routing reduces the area 184mm^{2}and Delay upto reduced 0.120ns . Synthesis results show that the area and critical path delay overheads are modest.**

***Keywords*—Minimum-Hop(MH) routing,RPM routing, Headfirst sliding routing .**

I.INTRODUCTION

Currently, microchips can only pass digital information in a very limited way — from either left to right or front to back, the researchers say. In the future, a 3D microchip would enable additional storage capacity on chips by allowing information to be spread across several layers instead of being compacted into one layer, as is currently the case.

This Long interconnects are becoming an increasingly important problem from both power and performance perspective. This motivates designers to adopt on-chip network-based communication infrastructures and three-dimensional (3D) designs where multiple device layers are stacked together. Considering the current trends towards increasing use of chip multiprocessing, it is timely to consider 3D chip multiprocessor design and memory networking issues.

The three-dimensional integration is a promising VLSI architecture that stack several smaller wafers or dies in order to reduce the wire length and wire delay, and three-dimensional Network-on-Chip (3-D NoC) [1] has been extensively including in terms of its network topology: The topology of an NOC specifies the physical organization of the interconnection network. It defines how nodes, switches and links are connected to each other [2][3][4], router architecture: Its responsible for correctly and efficiently routing packets[5][6][7], and routing strategy: It determines how data flows through the routers in the network and also defines the data transfer and applied switching techniques[8].

There has been considerable discussion in recent years on the benefits of 3-D silicon integration in which multiple device layers are stacked on top of each other with direct vertical interconnects tunneling through them [9] [10] [11] [12] [13]. 3-D integration promises to address many of the key challenges that arise from the semiconductor industry's relentless push into the deep Nano-scale regime. The increasing viability of 3-D technology has opened new opportunities for chip architecture innovations. One direction is in the extension of two-dimensional (2-D) tiled chip-multiprocessor architectures [14] [15] [16] [17] into three dimensions [18] [19]. Many proposed 2-D tiled chip-multiprocessor architectures have relied on a 2-D mesh network topology as the underlying communication fabric. Extending mesh-based tiled chip-multiprocessor architectures into three dimensions represents a natural progression for exploiting 3-D integration. The focus of this paper is on providing efficient routing for such 3-D Various interconnection techniques have been developed to connect multiple chips in a 3-D IC package: wire-bonding, micro-bump [20][21], wireless (e.g., capacitive- and inductive coupling) [22][23][24][25] between stacked dies, and through silicon via (TSV) [22][26] between stacked wafers. These 3-D IC technologies are compared in [6]. Many recent studies on 3-D IC architectures focus on micro-bump and TSV techniques that offer the highest level of interconnect density. On the other hand, as another 3-D integration technique, the inductive coupling can connect more than two examined dies without wire connections.

Toward this purpose, the vertical communication interfaces should be simplified, while arbitrary or customized topologies should be used for intra-chip networks; thus, we focus on mesh networks.static Time Division Multiple Access (TDMA) buses for the inter-chip communication. In this paper, we propose the Headfirst sliding routing scheme to overcome the delay problem and reduced area in simple static TDMA-based vertical buses. The static TDMA-based vertical buses grants a communication time-slot for different chips at the same time periodically, which means they are working with different periodic scheduling. For example, at a certain moment, vertical bus 0 gives a time-slot for chip 0, vertical bus 1 allows chip 2, and vertical bus 2 allows chip 1. At the next phase, vertical bus 0 gives a time-slot for chip 2, vertical bus 1 allows chip 0, and vertical bus 2 allows chip 1. Eachvertical bus behaves just like an elevator in an office building.

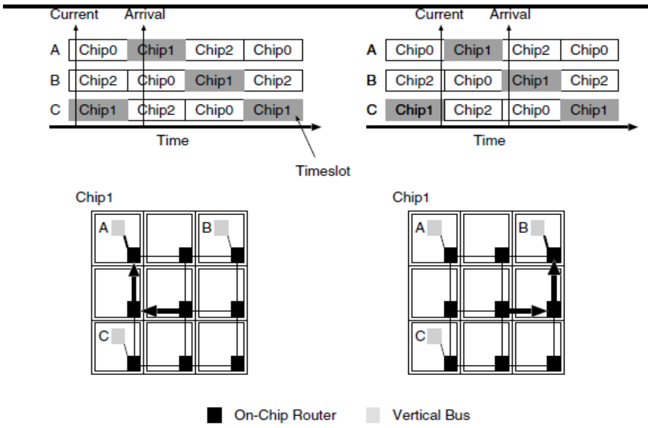
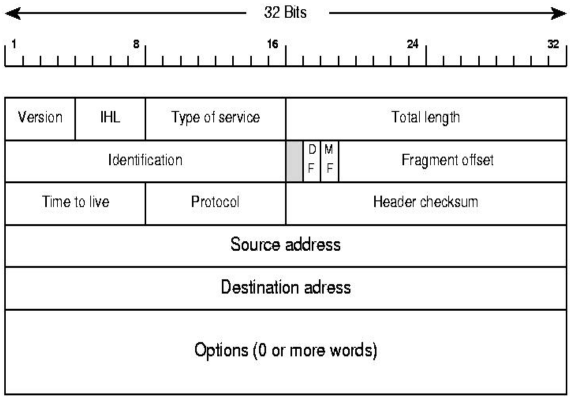

Current
Arrival
A Chip0 Chip1 Chip2 Chip0
B Chip2 Chip0 Chip1 Chip2
C Chip1 Chip2 Chip0 Chip1
Time
Timeslot
Chip1
A
B
C
On-Chip Router
Vertical Bus

Fig 1: Concept of Headfirst sliding routing

In concept of Headfirst sliding routing is after receiving the from 3D router switch then that data should be stored in the one of the communication time slots in the vertical bus, likewise one particular time send the more packets then this vertically connected TDMA buses gives the permission to communication time slots for different chips at same time. If send again more data then TDMA buses occupied in the next phase periodically.

For example in the Fig1 shows dark the chip 1 time slots because here consider chip 1 is the receives the packet from switch. When the data is depending on the current and arrival time then we concentration on our arrival time where appeared means which bus is allow the chip 1 and routs the packet towards the destination through the accepted bus (here accepted bus is A).

II.IPV4 PACKET HEADER



Version	IHL	Type of service	Total length		
Identification			D F	M F	Fragment offset
Time to live	Protocol		Header checksum		
Source address					
Destination adress					
Options (0 or more words)					

III. MINIMUM-HOP(MH) ROUTING

Minimum-hop (MH) routing and Headfirst sliding (HS) routing. MH routes packets using a minimal path between a source and a destination via an elevator. Our observation is that MH routing achieves a high saturated throughput while its zero-load communication waiting time or delay is longer than that of the dynamic TDMA (ideal case) due to the waiting time at switch. But here occur deadlock situation because without connecting virtual channels(VCs).

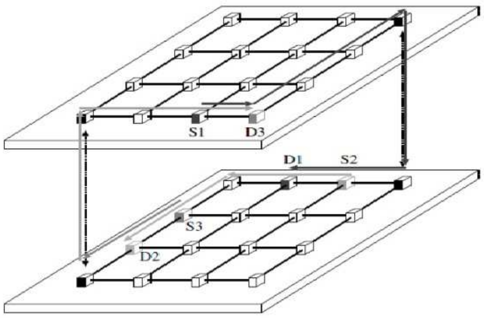


Fig 3:example of Deadlock situation

Minimum Hop Routing Packets are routed based on the following rules:

Case 1: If the source and destination are on the same chip, packets are routed based on arbitrary deadlock free routing on the chip (e.g., XY routing on 2-D mesh topology).

Case 2: If the source and destination are on different chips, packets are first routed to an elevator on the source chip, moved to the destination chip, and routed to the destination. An elevator is selected so that the hop count is minimized. Figure 2 illustrates an example of deadlock situation. Each chip employs 4 × 4 2-D mesh topology, in which XY routing is used for intra-packet transfers. In this case, S1 sends a message to D1, S2 sends a message to D2, and S3 sends a message to D3; thus they cause the cyclic dependency which introduces deadlocks.To reduce this deadlock virtual channels are added to each router.

IV.ROUTER IMPLEMENTATION

In this section, we discuss how 3D with Headfirst sliding router can be efficiently integrated into a typical on-chip router. We first explain how Headfirst sliding router can be made reduce delay and area.

a. RPM Router:

Fig. 5 shows the architecture of a typical 7-port router for 3-D mesh networks. But in the 2-D mesh networks have only with the addition of two extra ports for vertical communication.

At each input port, buffers are organized as separate FIFO queues, one for each VC. Flits entering the router are placed in one of these queues depending on their VC ID. The router is generally pipelined into five stages comprising *route computation, VC allocation, switch allocation, switch traversal and link traversal.*

The route computation stage determines the output port of a packet based on its destination. This is followed by VC allocation where packets acquire a virtual channel at the input of the downstream router. A packet that has acquired a VC arbitrates for the switch output port in the switch arbitration stage. Flits that succeed in switch arbitration traverse the crossbar before finally traversing the output link to reach the downstream router. Head flits proceed through all pipeline stages while the body and tail flits skip the route computation and VC allocation stages and inherit the output port and VC allocated to the head flit. The tail flit releases the reserved VC after departing the upstream router.

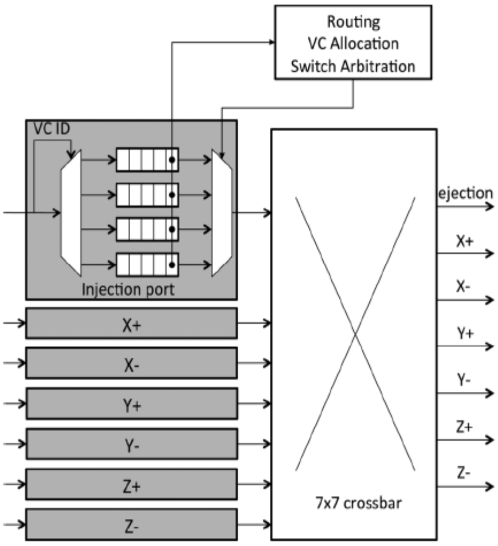
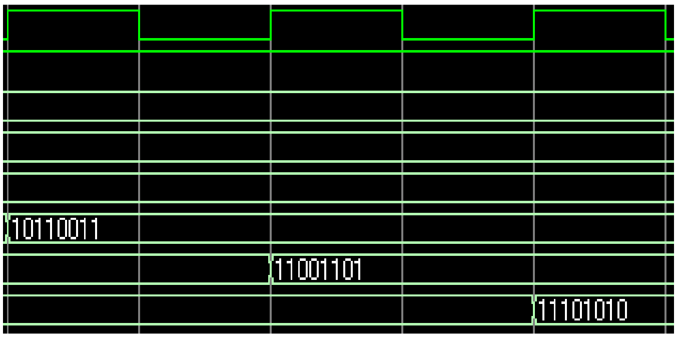


Fig 5: 3D router architecture



Too much delay problem in simple TDMA-based vertical buses. here given three channel data’s but three only consumed more delay and area. To overcome this area and delay problem “Headfirst sliding Routing concept” is introduced.

V. PROPOSED RPM ROUTER ARCHITECTURE

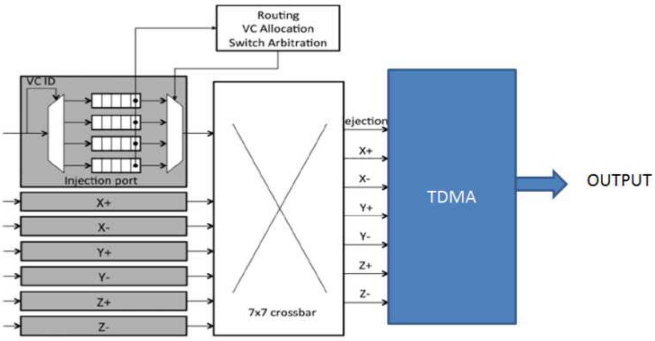


Fig 6:Proposed 3d router architecture

In the proposed router architecture have an advantages i.e reduced the delay ,area and power dissipation.
Headfirst Sliding Routing concept:

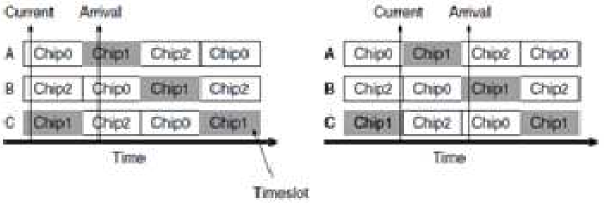
- we propose the Headfirst sliding routing scheme to overcome the simple static TDMA-based vertical buses. The static TDMA-based vertical buses grants a communication time-slot for different chips at the same time periodically, which means they are working with different periodic scheduling.
- Fortunately, a waiting time to obtain the time-slot of vertical bus (elevator) is predictable for each chip, thus a key design of packet routing is to select the best elevator that minimizes the waiting time.

TDMA (Headfirst Sliding Routing concept) is reduced the delay. if we compare with old paper (Randomized Partially-Minimal Routing:
Near-Optimal Oblivious Routingfor 3-D Mesh Networks ,page no.2092) and headfirst sliding routing concept.

POWER	AREA
3D ROUTER : 413.46mW	3D ROUTER: 626114mm$^{2.}$
HEADFIRST SLIDING ROUTING : 50.2mW	HEADFIRST SLIDING ROUTING : 184mm^{2}

Table :comparison between area and power.

VI. Headfirst Sliding Routing concept architecture



VII. MATHEMATICAL DESCRIPTION

Packets are first routed to an elevator on the source chip, moved to the destination chip, and routed to the destination. An elevator is selected so that the expected transfer time is minimized.

T is formulated as follows.

$T = RHsd + Twait$---(1)

where R is a flit transfer time at a router, Hsd is the number of hops from source to destination, and $Twait$ is an expected waiting time at an elevator.

$Twait$ is calculated as follows. First the arrival time of a packet to an elevator $Tarrive$ is calculated as follows, assuming no packet contentions.

$Tarrive = CurrentTime + RHsb$------------------ (2)

where Hsb is the number of hops from source to elevator, which is depending on the routing algorithm. The transfer start and finish times can be estimated based on this $Tarrive$.

Let $Talloc$ is a time-slot allocation time and $Tslot$ is the length of a time-slot. If a packet transfer start time is greater than or equal to $Talloc$ and a packet transfer finish time is less than $Talloc + Tslot$, $Twait$ is zero. Otherwise, $Twait$ is set to the next time-slot allocation time.

VIII. POWER AND AREA EVALUATION

In this section, we evaluate the power and area of a baseline 3-D router. To provide accurate comparisons, we implemented the baseline 3-D router with Headfirst sliding routing down to the gate level, and we used post-layout power and area results for our comparisons. In particular, the Verilog RTL implementation for the baseline 3-D router +Headfirst sliding routing was generated using modelsim SE 6.2c [-------], a fully-synthesizable parameterized router generator that implements an input-buffered pipelined virtual channel router. We consider a baseline 7-port router with 8 VCs per port, 5 flits/VC and a flit width of 16 bytes. For the 3D routers, we extended the Verilog design of the baseline router by incorporating the additional logic needed to implement Headfirst sliding routing. The router RTLs were synthesized with target version is xa3s250e-3tqg144.

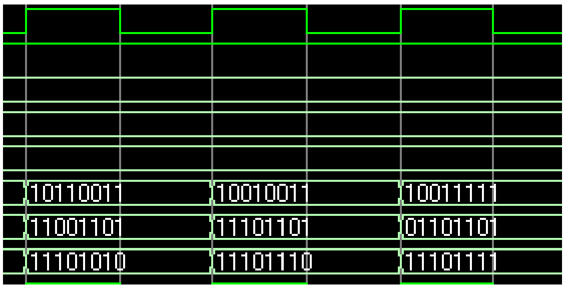
IX. EVALUATION

Port	7 input/output port
Buffer	7 flit
Routing	XYZ routing
Switching	Wormhole 2 virtual channels
Pipeline stage	Router computation, virtual channel allocation, switch allocation, switch traversal and link traversal
Flit size	128 bit

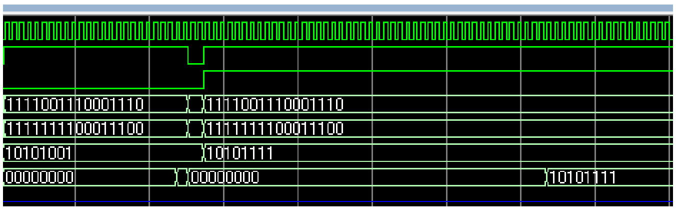
Table 1:Baseline Router

X. RESULTS

To used the virtual channels waiting time or delay would be reduced and also inter chip interconnects occupy the small chip area or reducing chip area.



And BUS not even check the error or packet loss but router would be very much helpful ERROR CHECKING and CORRECTION.



Results shows the 4X4 NOC Router. used two chips , both chips have 16 nodes. from the first chip out of 16 nodes packet used the only six nodes and from the second node out of 16 node used only five nodes. This means on the chips router routes the packet to destination used less nodes.

XI. CONCLUSION

As the demands on high performance and multi-function systems increase, vertically stacked 3DICs have the advantage is short communication distance between chips, leading to high data rate and low power consumption.In this paper, we proposed a new oblivious routing algorithm for 3-D mesh networks called RPM routing. Long interconnects are becoming an increasingly important problem from both power and performance . A wire-less approach that connects chips in vertical dimension has a great potential to customize interconnects or components in 3-D chip multiprocessors (CMPs). The Headfirst sliding routing scheme to overcome the simple static TDMA-based vertical buses.The result of the network performance showed that Headfirst Sliding Router reduces power and area , although Headfirst Sliding Router performs better than the normal 3D router at a high workload.
MH routing does not guarantee deadlock-freedom without virtual channels. To avoid deadlocks, two VCs are required for all the routers.

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